

CSH Consulting, LLC

**Signal Integrity Consulting
April 2022**

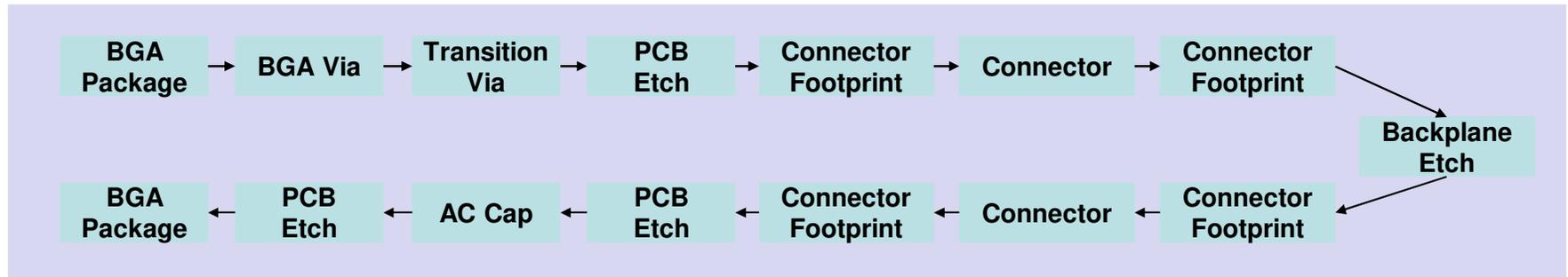
Overview

- High Speed Serial Channel Modeling
 - 25Gbps Ethernet, 56G PAM-4, PCIe GenX, Fibre Channel, SAS, USB
 - Anything over 2Gb/s requiring frequency domain simulation and modeling.
- High Speed Memory Simulation
 - DDR2, DDR3, DDR4
 - Clock, Address, Data, Strobe
 - Buffer Strengths, On Die Termination, Topology, Waveform Integrity, Setup and Hold Mask Evaluations for DQ and Command/Control/Address.
 - DQ Rx Eye Mask for DDR4
- Power Integrity Simulation
 - DC Analysis and Frequency Response Analysis of Power Planes
 - Decoupling Capacitor Optimization
- CAD Guidelines
 - Concise recommendations for PCB Layout based on Pre-Layout Simulations.

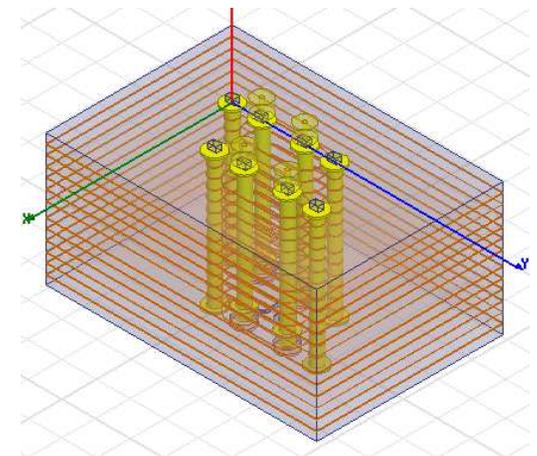
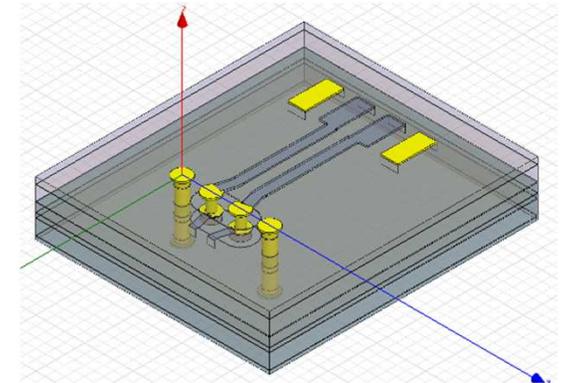
Simulation Capability

- Software Resources
 - Ansys HFSS
 - 3D Modeling of structures (vias, AC Caps, BGAs, Connectors)
 - 3D Modeling of pcb etch.
 - In-house automation ensures faster response and consistency
 - Ansys SIwave
 - Power Plane Voltage Drop simulation
 - Power Plane Frequency analysis and decoupling capacitor optimization
 - Keysight ADS
 - Statistical Eye simulation using IBIS-AMI Models
 - HSpice
 - Time Domain Simulation using IBIS
 - Frequency Domain Simulation
 - Concatenation of S-Parameters

Channel Modeling - Process and Tools



- **Link Models** created in HSpice
 - Cascaded S-parameters of connector, footprint, etch
- **Connector Models**
 - Provided by Connector Vendor in Touchstone format.
- **PCB Footprints**
 - Simulated in Ansoft HFSS
- **PCB Etch Models**
 - De-Embedded S-parameter Model generated in HFSS



Passive Channel Design Drivers

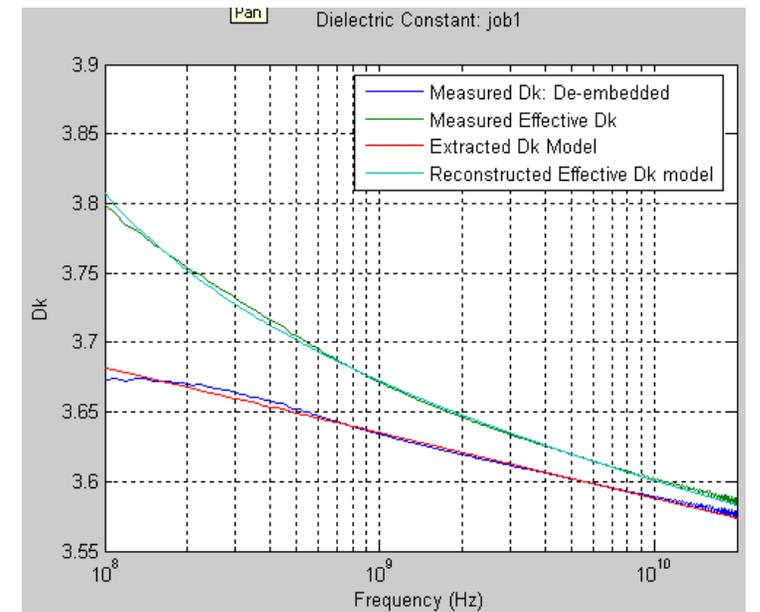
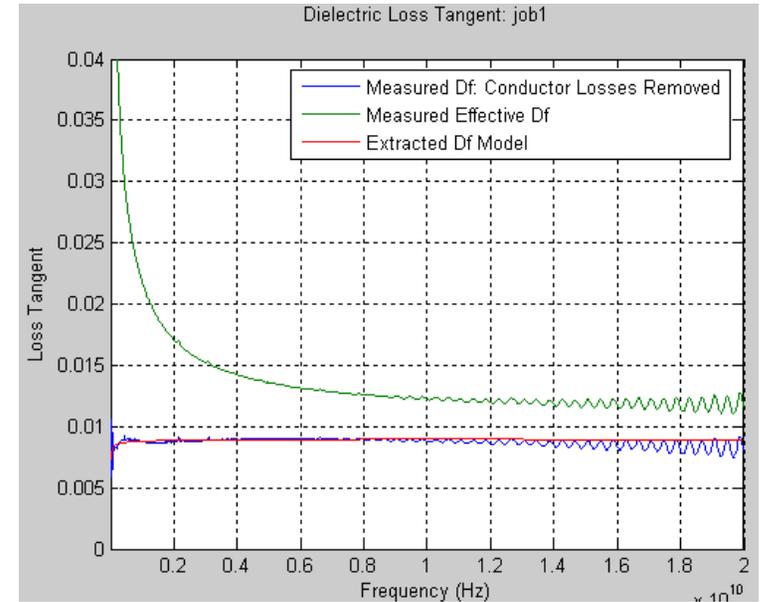
- **Insertion Loss**
 - Driven by PCB material property and via stubs.
- **Return Loss**
 - Driven by Impedance mismatches mainly arising in component footprints.
- **Crosstalk**
 - Unwanted electromagnetic coupling between traces, vias and connector contacts.
- **Skew**
 - Driven by routing, connector, and PCB laminate material.
- **Common Mode Conversion and EMI**
 - Driven by unbalanced differential pairs in routing and connectors.

PCB Material Property Extraction From Measurements

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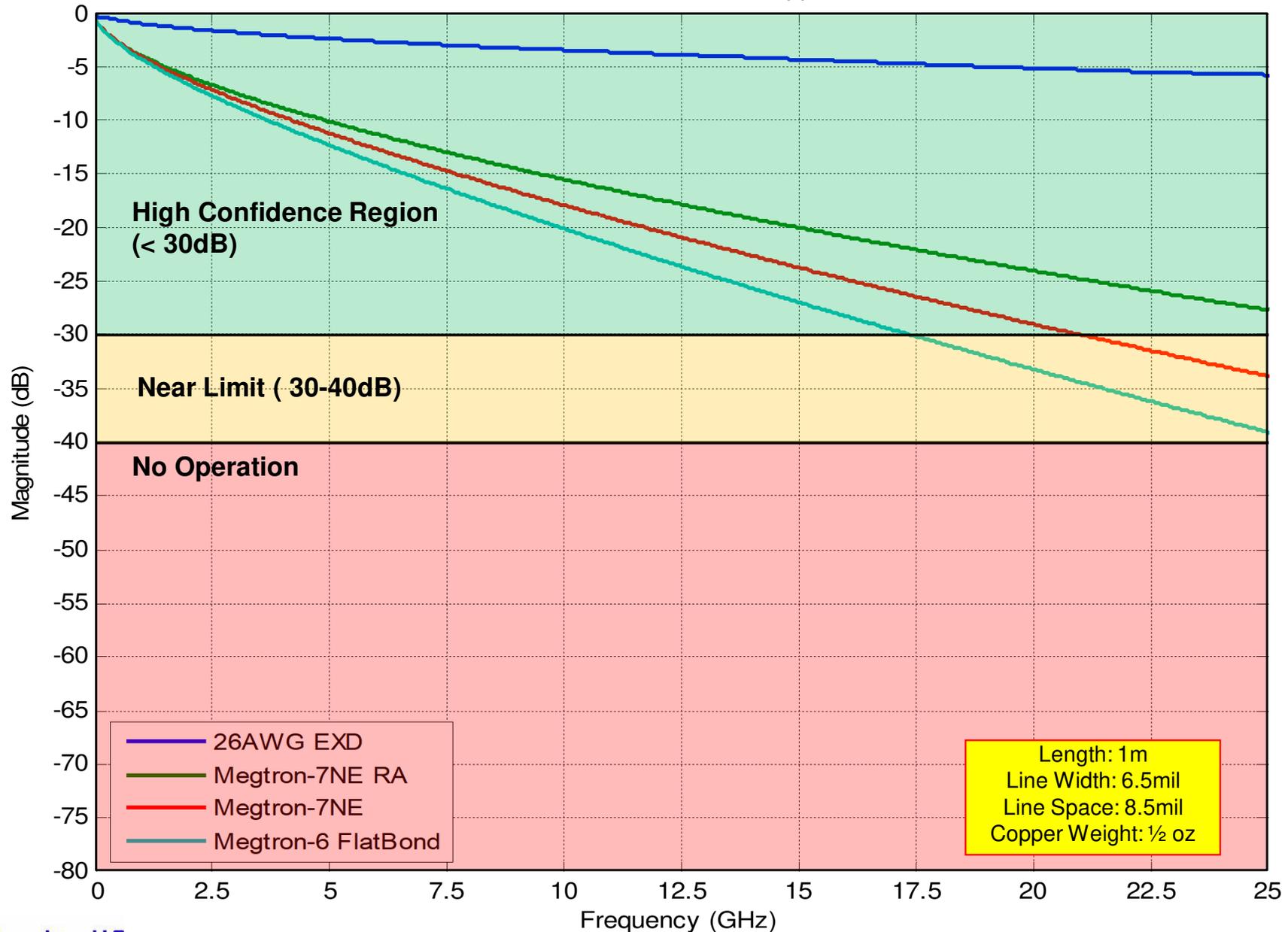
*****
..... Model Extraction Report
-----
frequency ..... Dk ..... Loss Tangent
-----
100 MHz ..... 3.68 ..... 0.00835
500 MHz ..... 3.65 ..... 0.00871
1 GHz ..... 3.64 ..... 0.00880
2.5 GHz ..... 3.62 ..... 0.00889
5 GHz ..... 3.60 ..... 0.00894
10 GHz ..... 3.59 ..... 0.00896
-----
Approx. Group Delay = 160.654092 pS/inch
-----
..... Model Extraction Confidence
-----
1.) R-squared error of reconstructed effective Dk from
100 MHz to 10 GHz: R^2 = 0.036487 %
2.) Confidence of reconstructed effective Dk
100 MHz to 10 GHz: 99.963513 %
*****

```



Insertion Loss vs PCB Material

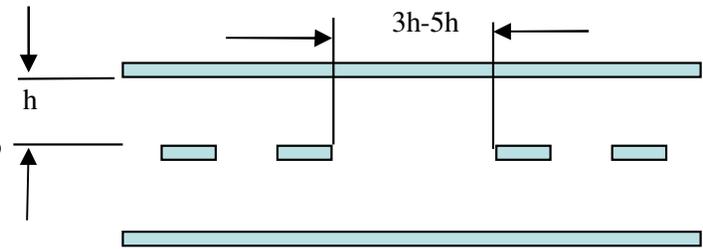
Loss Characteristic of 1m of Copper Medium



Crosstalk Sources

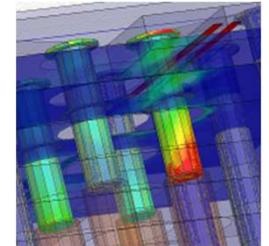
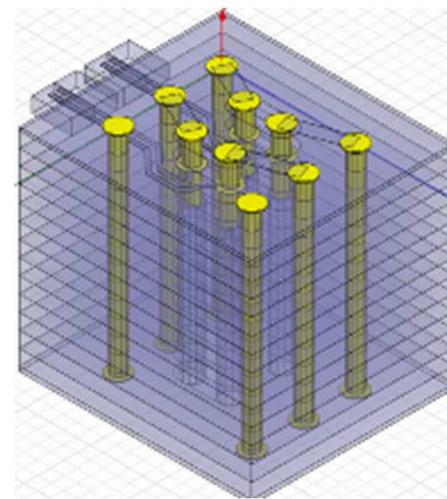
1. Between Differential Pair Traces

- Crosstalk Target $\leq -50\text{dB}$



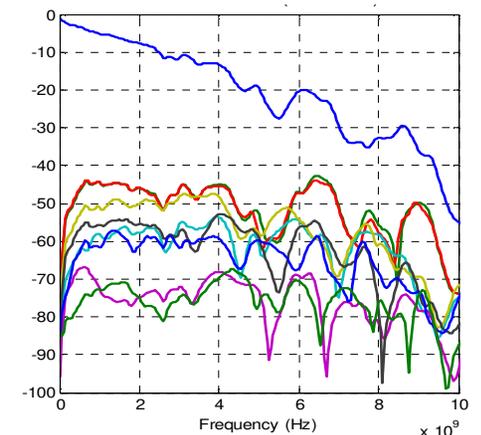
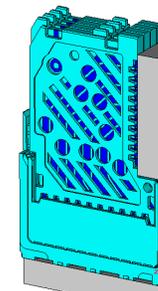
2. Between Vias in Footprint

- Simulate and Tune
 - Antipad shapes
 - Drill size
 - Pad Size
 - Backdrill Depth



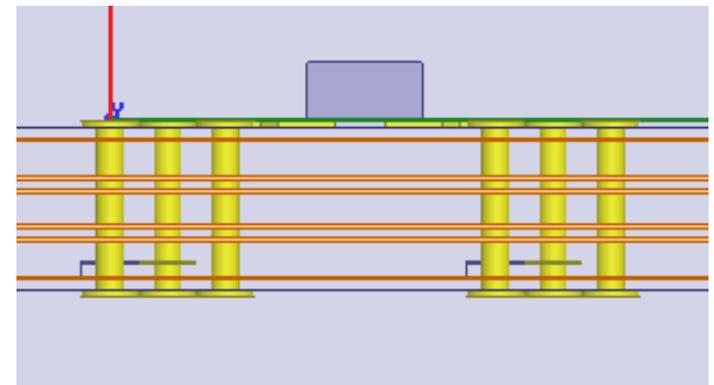
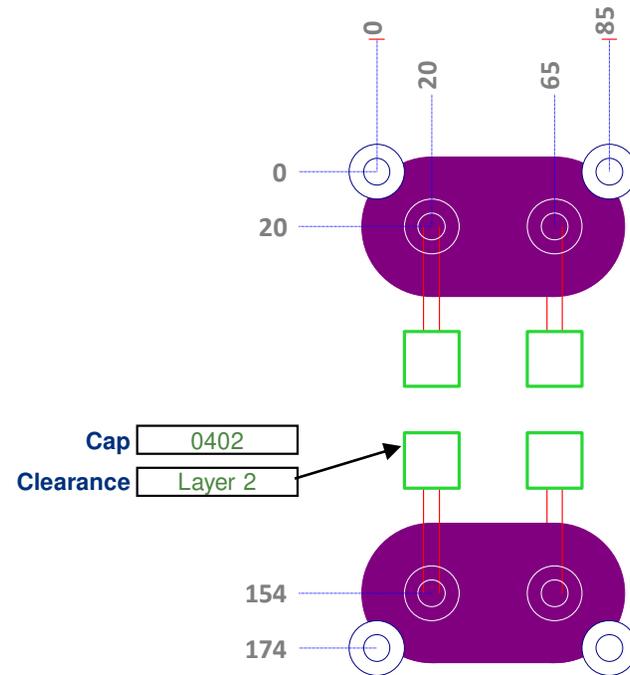
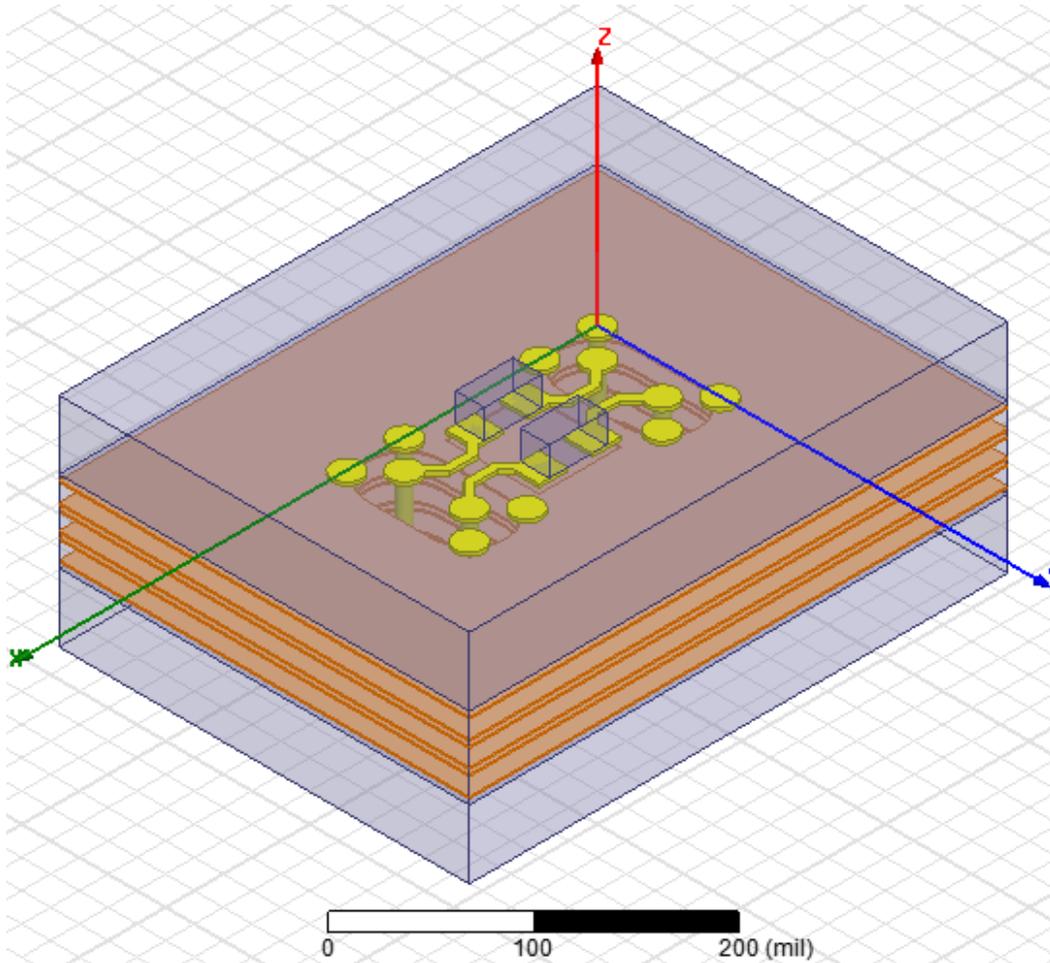
3. Within Connectors

- Simulate and tune conductor geometry, plastic materials and return paths.



HFSS 3D Model Example

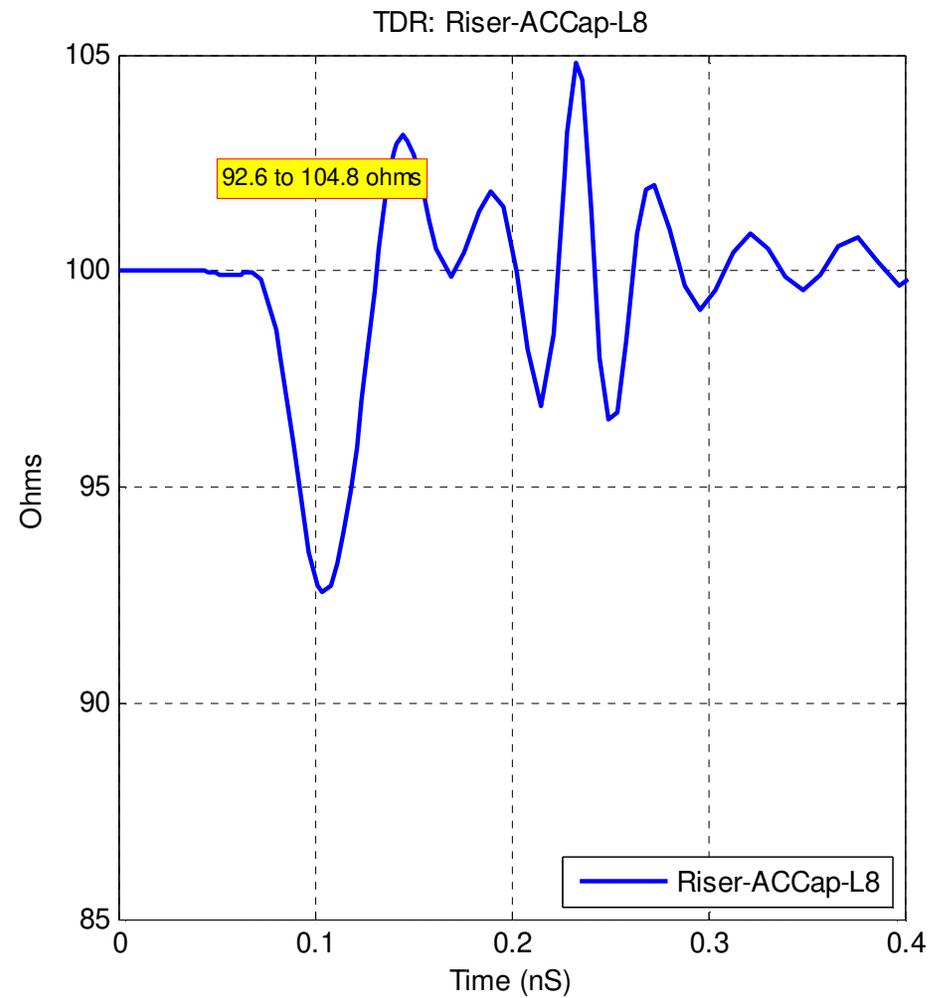
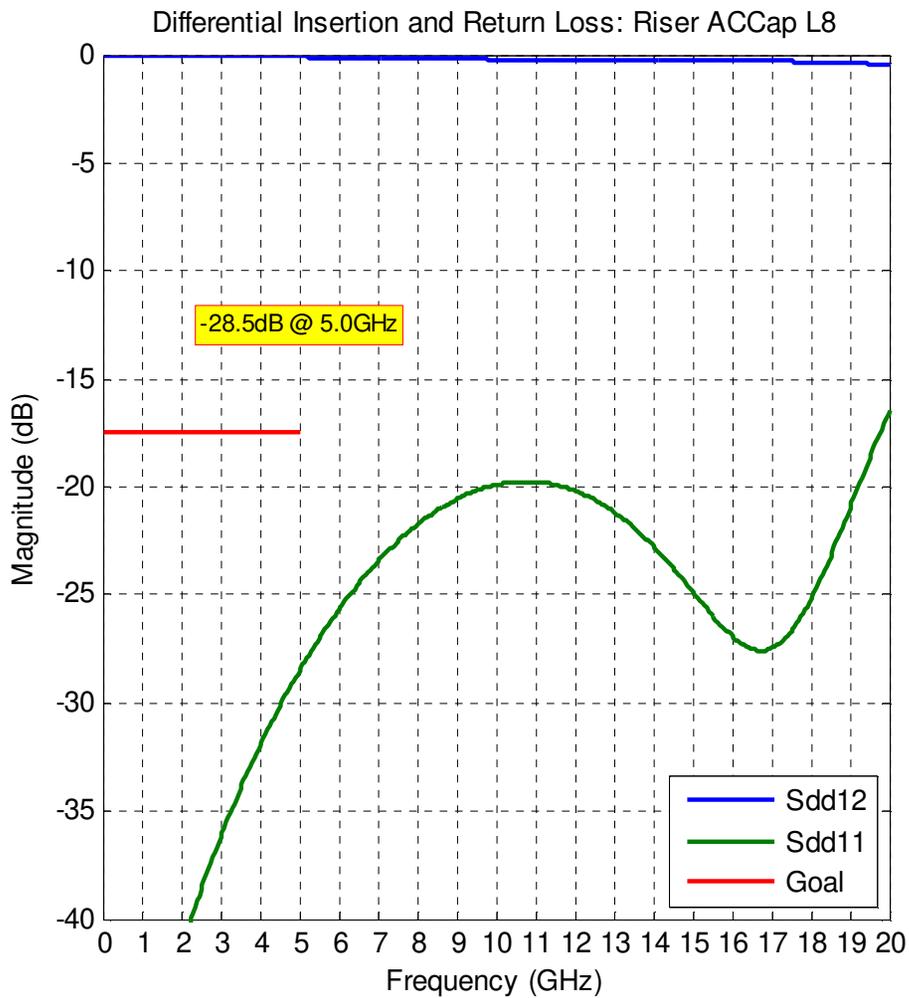
DC Blocking Capacitor Example



Finished Dia	5.8mil	Diff Port Zo	100	Material	Megtron-4
Drill Dia	9.8mil	Layer Escape	8	Dk	3.8
Pad Dia	20.0mil	Line Width	4.25mil	Df	0.01
Antipad Dia	51.0mil	EtchBack	0.1mil	Layers	10
Oval Dogbone	51.0mil	Line Space	11.5mil	Thickness	61.4 mil
		Anti Line Width	4.25mil	Max Freq.	20 GHz
				Adapt Freq.	10 GHz

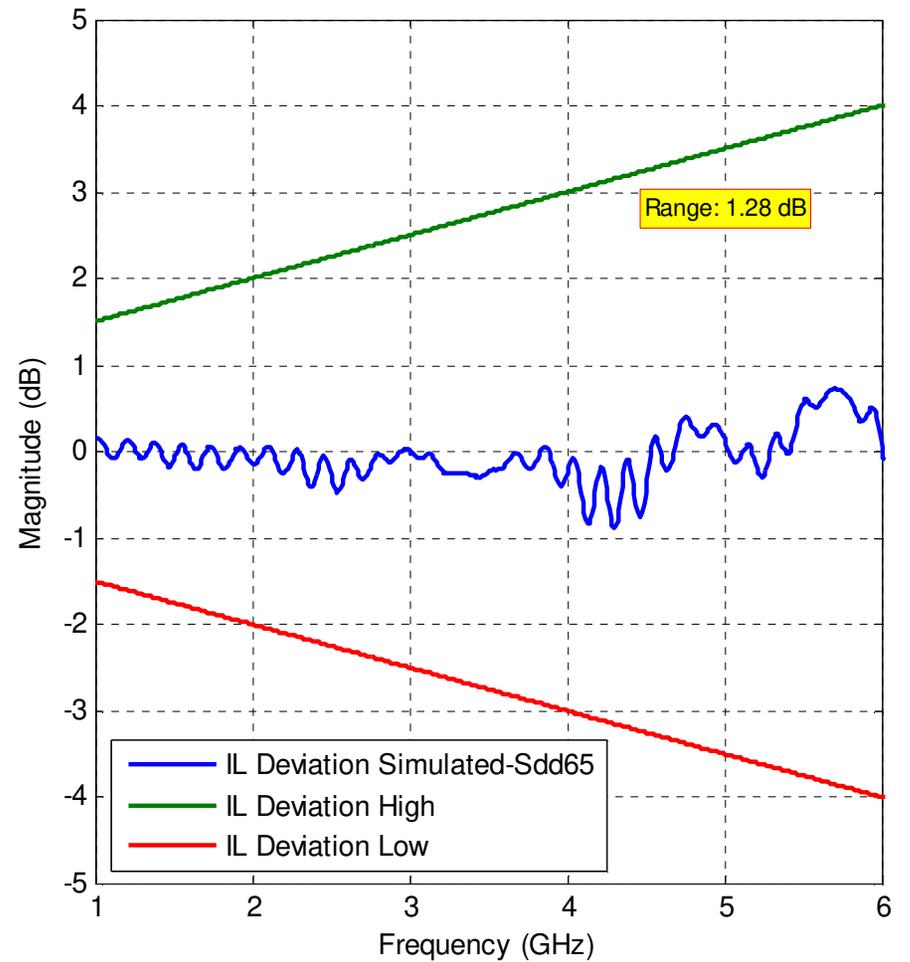
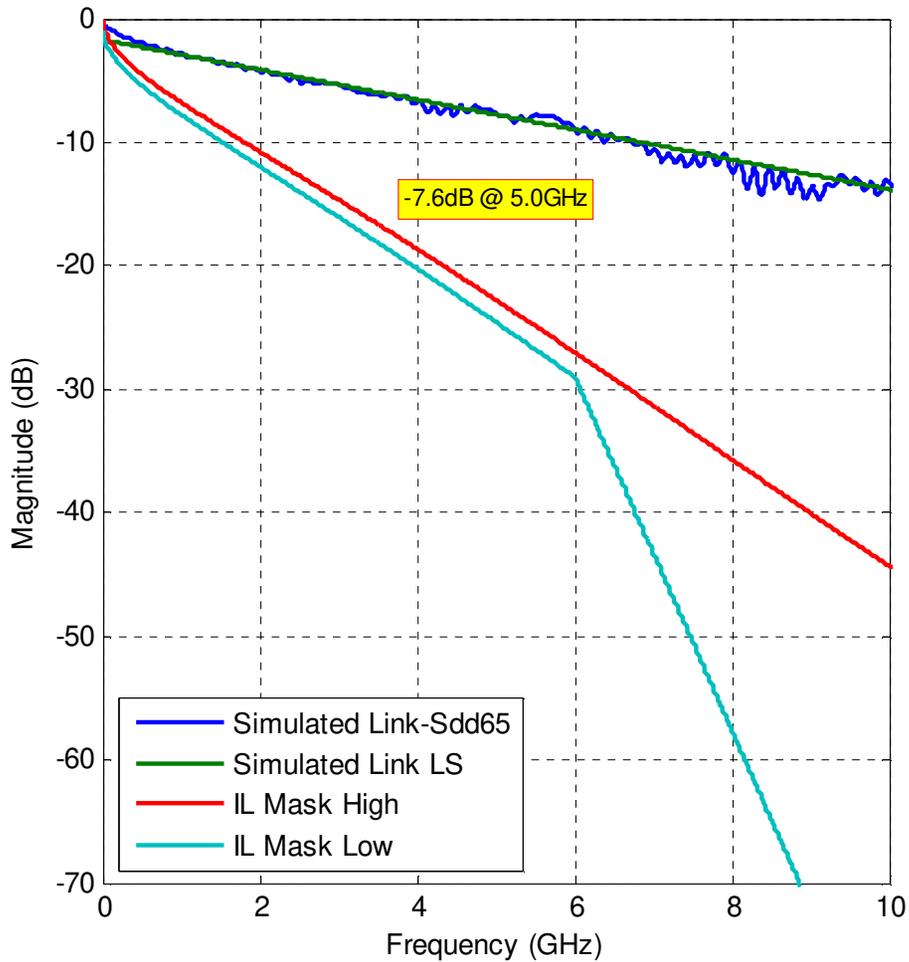
DC Blocking Capacitor Example Results

Insertion Loss, Return Loss and TDR

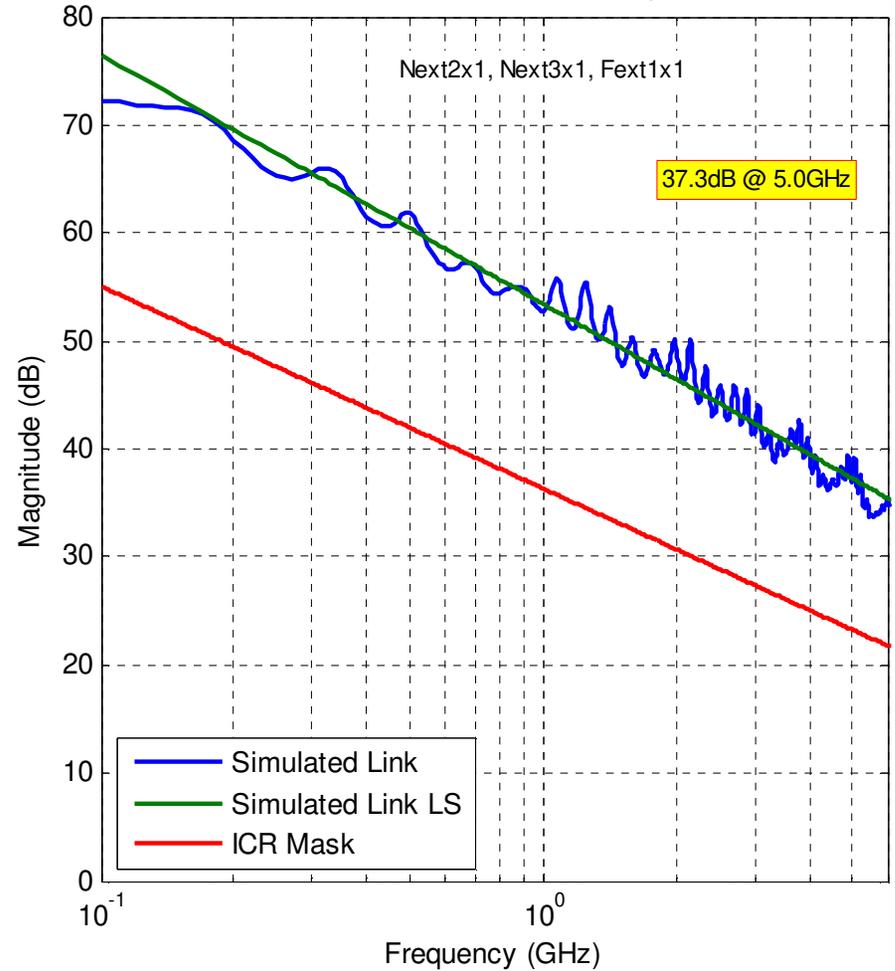
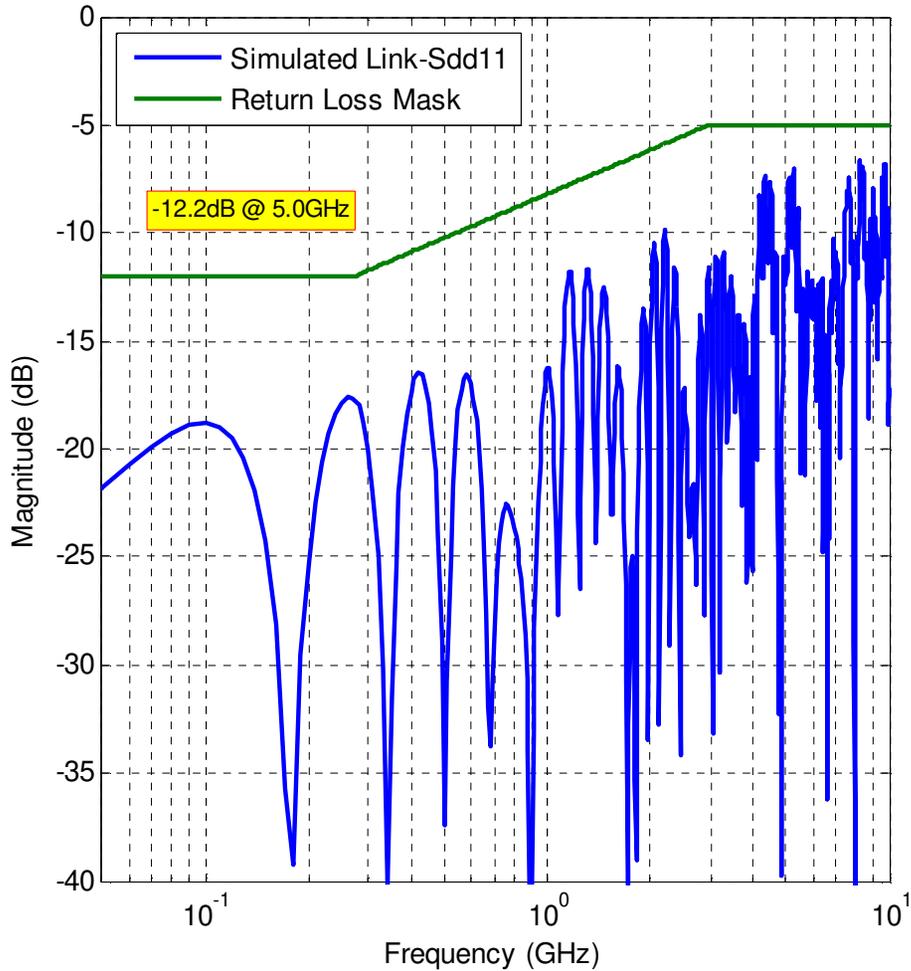


Frequency Domain Mask Plot Examples

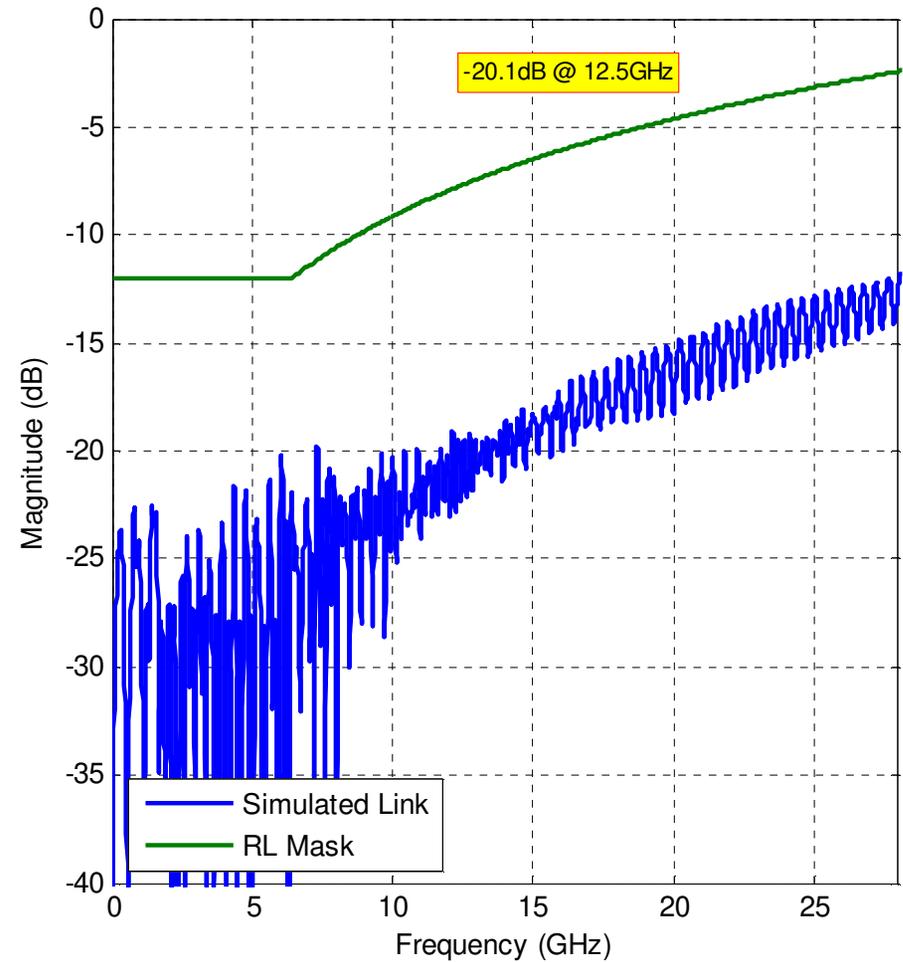
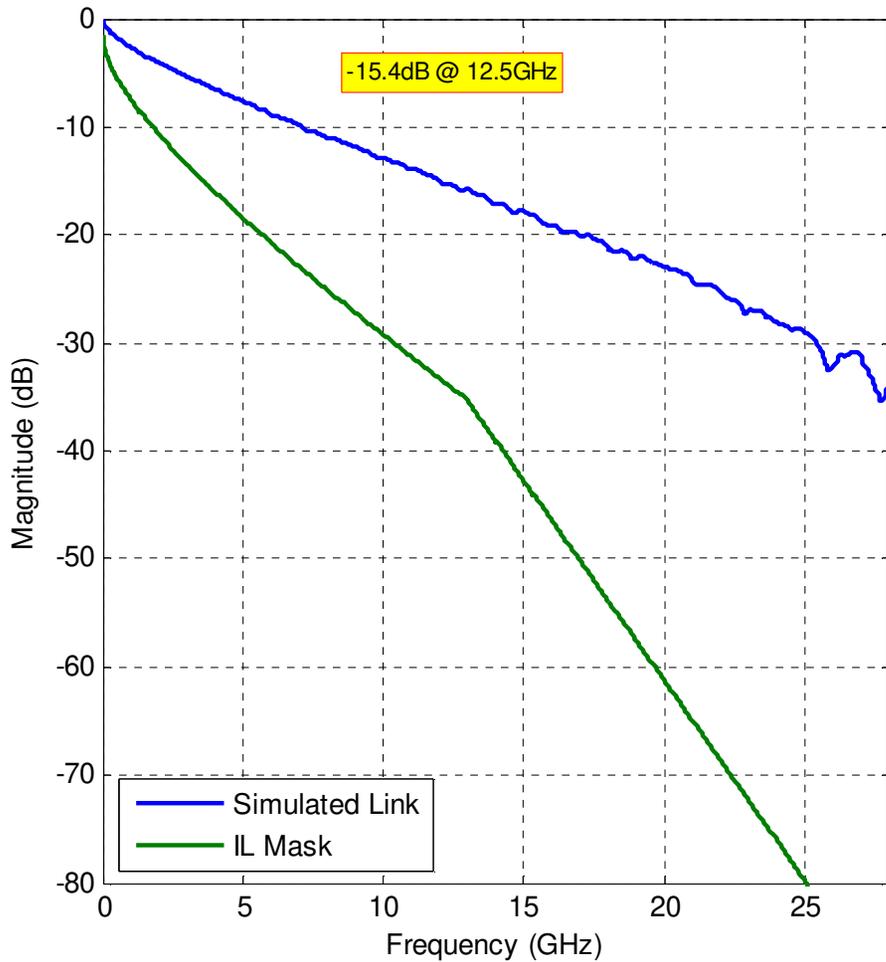
IEEE 802.3ap KR (10Gbps): Insertion Loss and ILD Channel Example



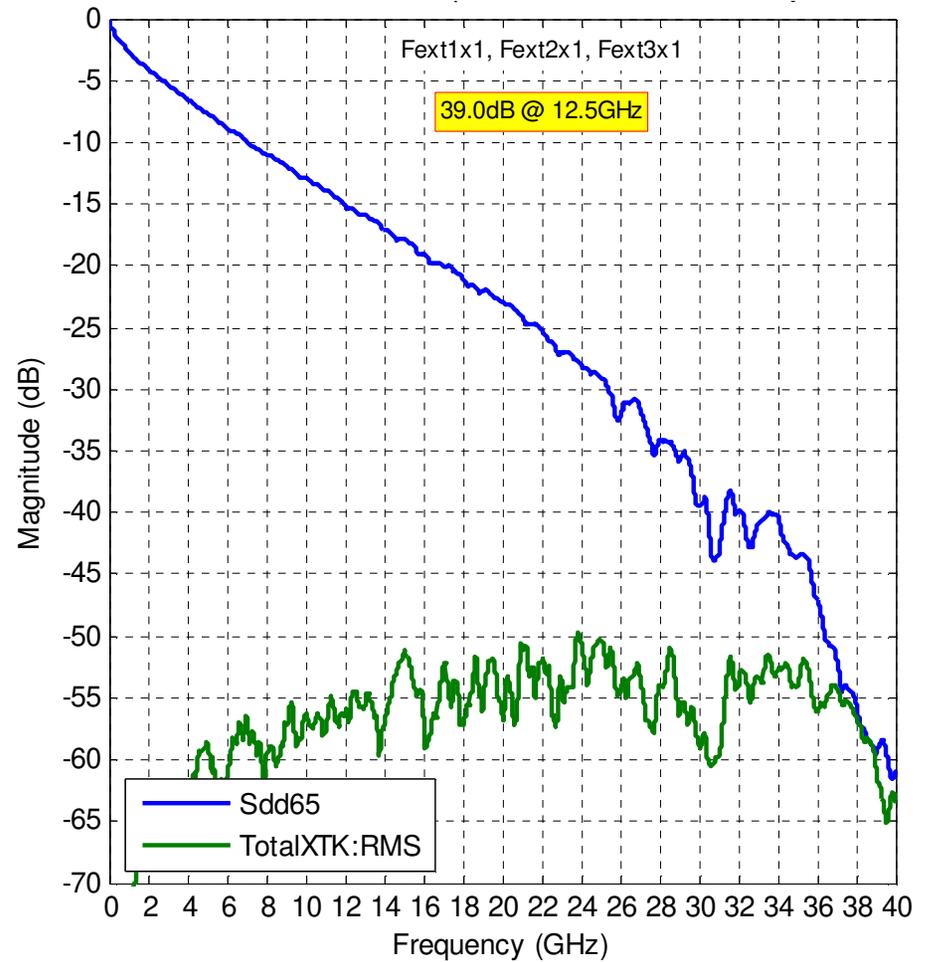
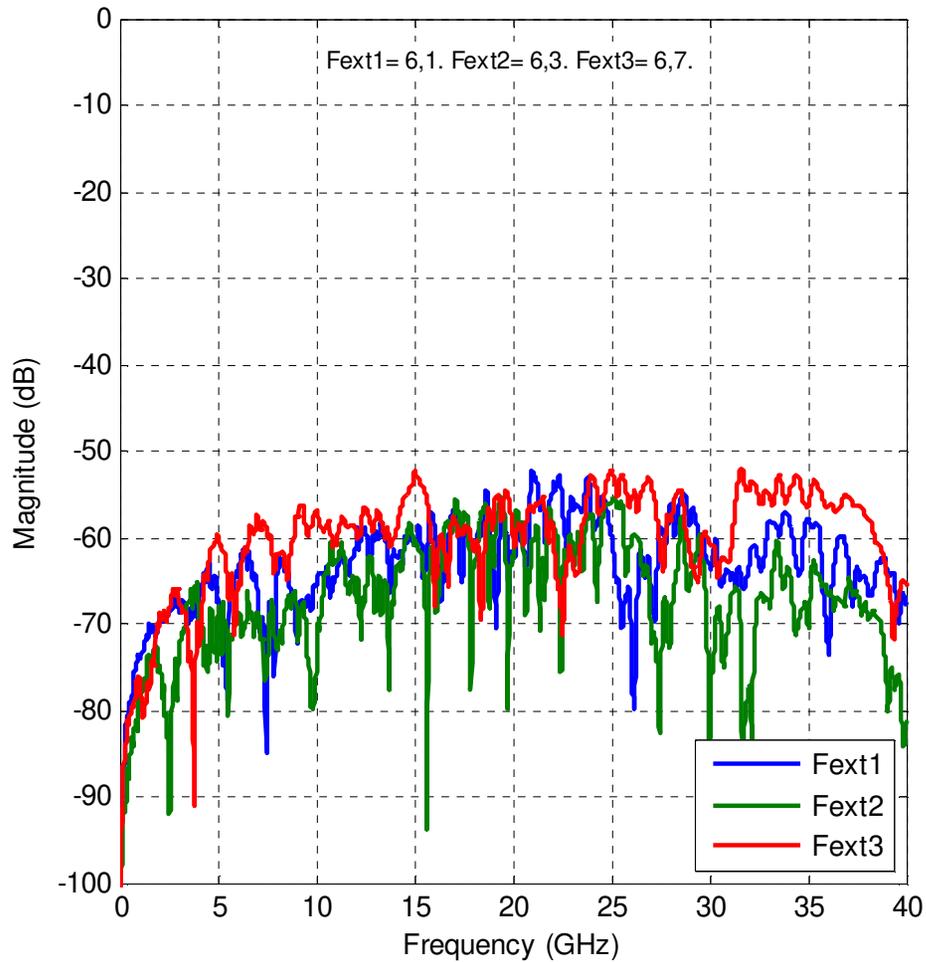
IEEE 802.3ap KR (10Gbps): Return Loss and ICR Channel Example



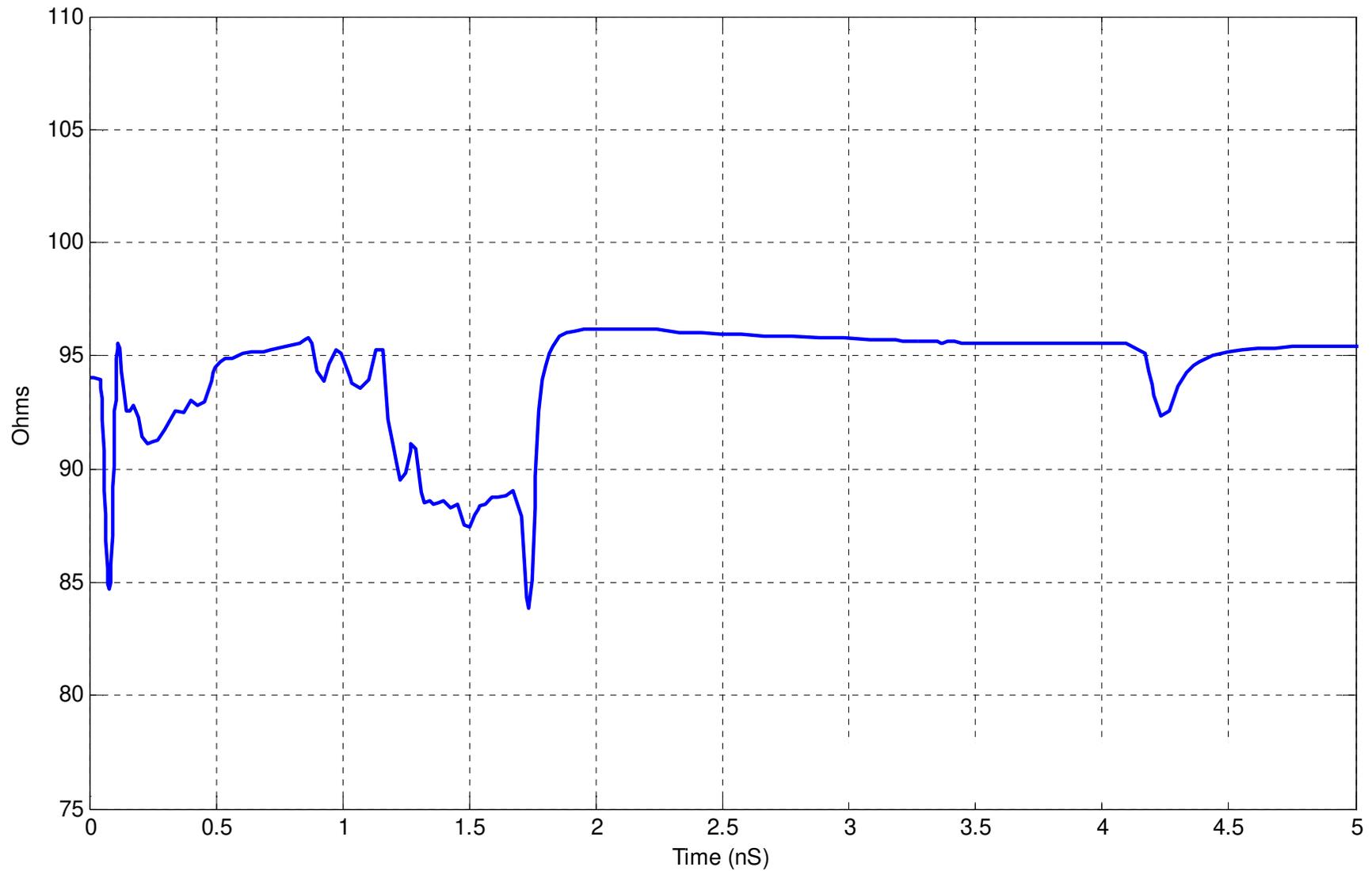
IEEE 802.3bj (25Gbps) Insertion and Return Loss Channel Example



IEEE 802.3bj (25Gbps) Crosstalk and ICR Channel Example

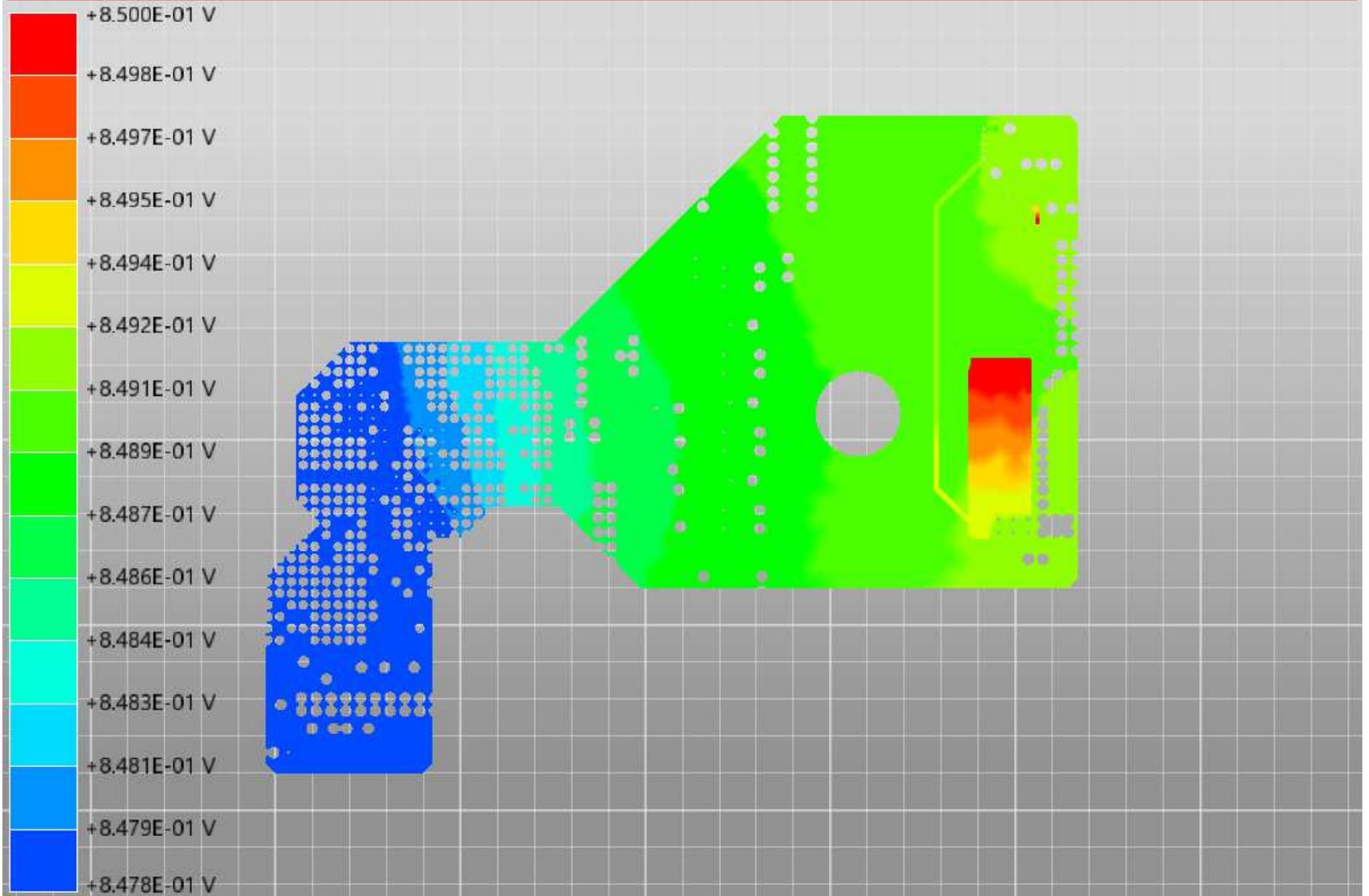


Channel TDR Channel Example



Power Integrity Example

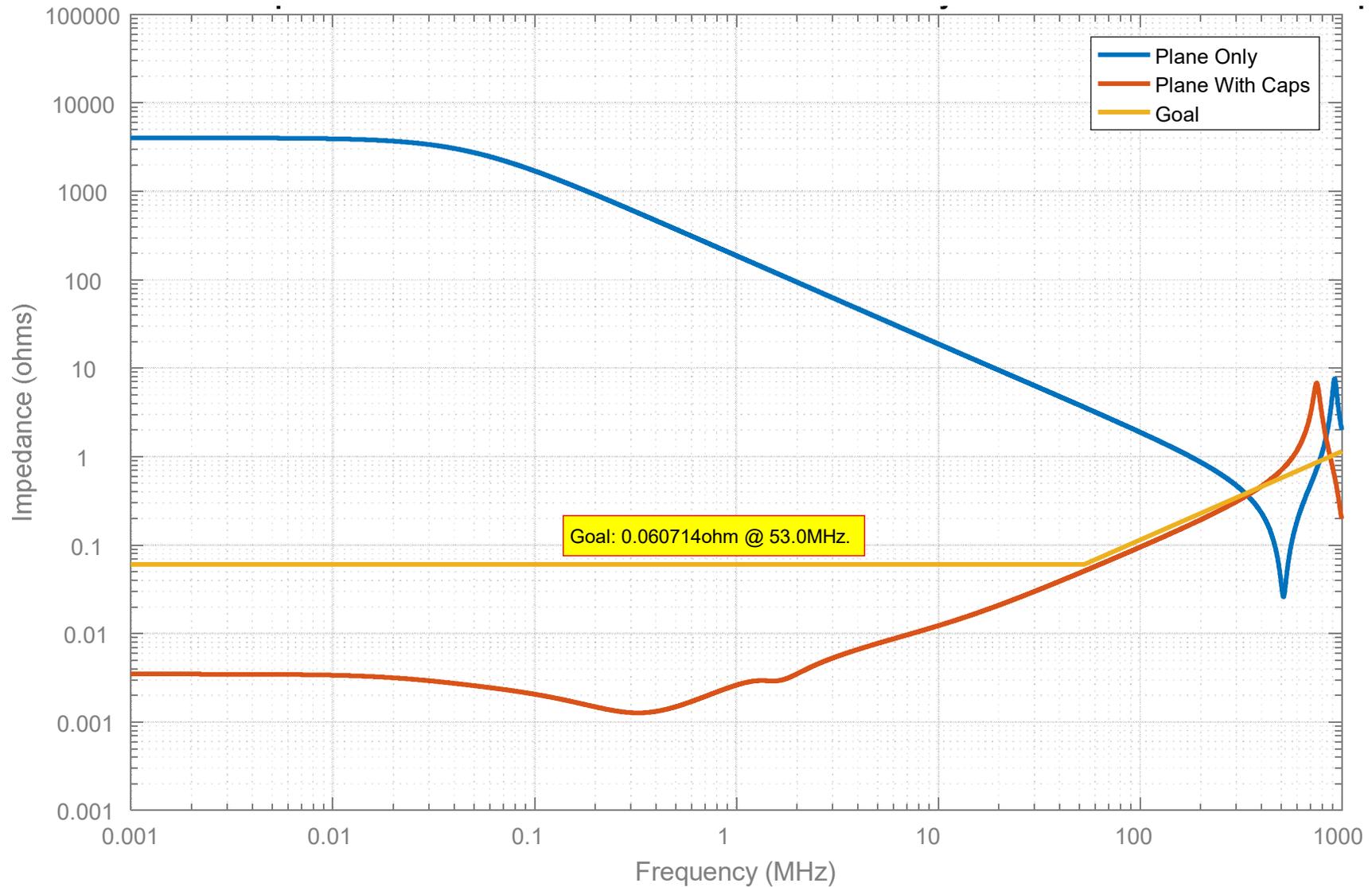
SIwave: Power Plane Voltage Drop



Via Current Summary Table:

Via	Net	x (mils)	y (mils)	Current / A	Limit / A	Pass / Fail
Via 508 (top-layer09_pwr)	POP85V	3.5550e+03	3.6250e+03	6.065851023113e-01	4.560367311877e+00	Pass
Via 482 (top-layer09_pwr)	POP85V	3.4550e+03	2.7850e+03	2.016381705431e-01	4.560367311877e+00	Pass
Via 498 (top-layer09_pwr)	POP85V	3.4950e+03	2.7850e+03	1.506142530358e-01	4.560367311877e+00	Pass
Via 497 (top-layer09_pwr)	POP85V	3.4550e+03	2.7500e+03	1.438979466836e-01	4.560367311877e+00	Pass
Via 507 (top-layer09_pwr)	POP85V	3.5350e+03	2.7850e+03	1.279233667954e-01	4.560367311877e+00	Pass
Via 483 (top-layer09_pwr)	POP85V	3.4950e+03	2.7500e+03	9.081182635109e-02	4.560367311877e+00	Pass
Via 506 (top-layer09_pwr)	POP85V	3.5350e+03	2.7500e+03	7.127225092733e-02	4.560367311877e+00	Pass
Via 1204 (top-layer02_gnd)	DGND	2.1730e+03	3.2150e+03	2.374140673540e-02	2.918635079602e+00	Pass
Via 1182 (top-layer02_gnd)	DGND	1.9840e+03	3.2780e+03	2.240853326091e-02	2.918635079602e+00	Pass
Via 829 (top-layer02_gnd)	DGND	2.0785e+03	3.3095e+03	2.196830183154e-02	2.918635079602e+00	Pass
Via 1147 (top-layer02_gnd)	DGND	2.2044e+03	2.4906e+03	2.134441722345e-02	2.918635079602e+00	Pass
Via 1145 (top-layer02_gnd)	DGND	2.1415e+03	3.2780e+03	2.126396269246e-02	2.918635079602e+00	Pass
Via 1215 (top-layer02_gnd)	DGND	2.2359e+03	3.1205e+03	1.964226941563e-02	2.918635079602e+00	Pass
Via 1204 (layer02_gnd-layer04_gnd)	DGND	2.1730e+03	3.2150e+03	1.960504603071e-02	2.918635079602e+00	Pass
Via 1145 (layer02_gnd-layer04_gnd)	DGND	2.1415e+03	3.2780e+03	1.810695599860e-02	2.918635079602e+00	Pass
Via 829 (layer02_gnd-layer04_gnd)	DGND	2.0785e+03	3.3095e+03	1.808692576007e-02	2.918635079602e+00	Pass
Via 1182 (layer02_gnd-layer04_gnd)	DGND	1.9840e+03	3.2780e+03	1.800920462244e-02	2.918635079602e+00	Pass
Via 1212 (top-layer02_gnd)	DGND	2.2044e+03	3.3094e+03	1.784221768812e-02	2.918635079602e+00	Pass
Via 1159 (top-layer02_gnd)	DGND	2.1100e+03	2.5220e+03	1.739799617351e-02	2.918635079602e+00	Pass
Via 1233 (top-layer02_gnd)	DGND	2.2359e+03	3.2465e+03	1.684444028602e-02	2.918635079602e+00	Pass
Via 1144 (top-layer02_gnd)	DGND	2.1100e+03	3.3409e+03	1.663374716941e-02	2.918635079602e+00	Pass
Via 1204 (layer04_gnd-layer06_gnd)	DGND	2.1730e+03	3.2150e+03	1.643795816182e-02	2.918635079602e+00	Pass
Via 1176 (top-layer02_gnd)	DGND	2.2044e+03	2.6480e+03	1.626761146039e-02	2.918635079602e+00	Pass
Via 1145 (layer04_gnd-layer06_gnd)	DGND	2.1415e+03	3.2780e+03	1.555084417122e-02	2.918635079602e+00	Pass
Via 1215 (layer02_gnd-layer04_gnd)	DGND	2.2359e+03	3.1205e+03	1.537469688342e-02	2.918635079602e+00	Pass
Via 1212 (layer02_gnd-layer04_gnd)	DGND	2.2044e+03	3.3094e+03	1.530524848390e-02	2.918635079602e+00	Pass
Via 799 (top-layer02_gnd)	DGND	2.0470e+03	3.2150e+03	1.526744007770e-02	2.918635079602e+00	Pass
Via 829 (layer04_gnd-layer06_gnd)	DGND	2.0785e+03	3.3095e+03	1.515363434602e-02	2.918635079602e+00	Pass
Via 1147 (layer02_gnd-layer04_gnd)	DGND	2.2044e+03	2.4906e+03	1.494344002332e-02	2.918635079602e+00	Pass
Via 1182 (layer04_gnd-layer06_gnd)	DGND	1.9840e+03	3.2780e+03	1.475873778530e-02	2.918635079602e+00	Pass
Via 1103 (top-layer02_gnd)	DGND	1.3856e+03	3.3094e+03	1.473474655680e-02	2.918635079602e+00	Pass
Via 1233 (layer02_gnd-layer04_gnd)	DGND	2.2359e+03	3.2465e+03	1.467950621358e-02	2.918635079602e+00	Pass
Via 1144 (layer02_gnd-layer04_gnd)	DGND	2.1100e+03	3.3409e+03	1.457576947778e-02	2.918635079602e+00	Pass
Via 1202 (top-layer02_gnd)	DGND	2.1415e+03	2.6165e+03	1.448245942769e-02	2.918635079602e+00	Pass
Via 1204 (layer06_gnd-layer08_gnd)	DGND	2.1730e+03	3.2150e+03	1.398827965619e-02	2.918635079602e+00	Pass
Via 1145 (layer06_gnd-layer08_gnd)	DGND	2.1415e+03	3.2780e+03	1.347144113496e-02	2.918635079602e+00	Pass
Via 1176 (layer02_gnd-layer04_gnd)	DGND	2.2044e+03	2.6480e+03	1.344922013859e-02	2.918635079602e+00	Pass
Via 1159 (layer02_gnd-layer04_gnd)	DGND	2.1100e+03	2.5220e+03	1.332881502947e-02	2.918635079602e+00	Pass
Via 1212 (layer04_gnd-layer06_gnd)	DGND	2.2044e+03	3.3094e+03	1.320783698093e-02	2.918635079602e+00	Pass
Via 799 (layer02_gnd-layer04_gnd)	DGND	2.0470e+03	3.2150e+03	1.308301466434e-02	2.918635079602e+00	Pass
Via 1018 (top-layer02_gnd)	DGND	1.3541e+03	2.4591e+03	1.305067818526e-02	2.918635079602e+00	Pass
Via 829 (layer06_gnd-layer08_gnd)	DGND	2.0785e+03	3.3095e+03	1.289972886506e-02	2.918635079602e+00	Pass
Via 1119 (top-layer02_gnd)	DGND	1.3856e+03	2.5850e+03	1.283685563592e-02	2.918635079602e+00	Pass
Via 1233 (layer04_gnd-layer06_gnd)	DGND	2.2359e+03	3.2465e+03	1.280010370320e-02	2.918635079602e+00	Pass
Via 1132 (top-layer02_gnd)	DGND	1.5430e+03	3.3094e+03	1.279990575829e-02	2.918635079602e+00	Pass
Via 1155 (top-layer02_gnd)	DGND	1.9525e+03	2.5220e+03	1.279976466463e-02	2.918635079602e+00	Pass
Via 1144 (layer04_gnd-layer06_gnd)	DGND	2.1100e+03	3.3409e+03	1.275043594595e-02	2.918635079602e+00	Pass
Via 1160 (top-layer02_gnd)	DGND	1.8265e+03	3.2780e+03	1.271415093956e-02	2.918635079602e+00	Pass
Via 1211 (top-layer02_gnd)	DGND	2.2359e+03	3.0890e+03	1.264246173780e-02	2.918635079602e+00	Pass
Via 1129 (top-layer02_gnd)	DGND	1.3856e+03	3.1520e+03	1.262944407797e-02	2.918635079602e+00	Pass

Power Plane Impedance vs. Frequency



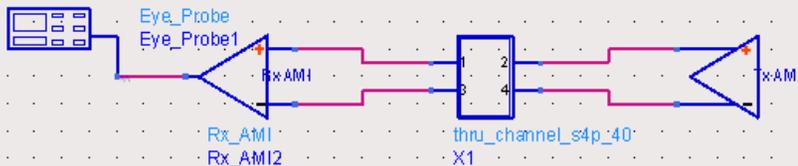
Statistical Eye Example

ADS Schematic: 1 Million Bit-By-Bit Simulation

Tx_AMI
Tx_AMI1
ComponentName="stratix_v_gx_tx"
PinName="10"
ModelName="stratix5_gx_tx_100_7"
DataTypeSelector=Fast
UsePkg=yes
CacType=Typ
BitRate=1.25 Gbps
Mode=Maximal Length LFSR
Tap="10001110"
Seed="10101010"
BitSequence="10101010"
NumberTimePPerUI=
AMlvarName[1]=Ignore_Bits
AMlvarName[2]=Max_Init_Aggressors
AMlvarName[3]=Init_Returns_Impulse
AMlvarName[4]=Use_Init_Output
AMlvarName[5]=GetWave_Exists
AMlvarName[6]=lvod
AMlvarName[7]=tap1
AMlvarName[8]=tap2
AMlvarName[9]=pretap
AMlvarName[10]=invTap2
AMlvarName[11]=invpretap
AMlvarName[12]=protocol
AMlvarName[13]=slew
AMlvarName[14]=Rterm
AMlvarName[15]=Process
AMlvarName[16]=Debug
AMlvarValue[3]=True
AMlvarValue[4]=False
AMlvarValue[5]=True
AMlvarValue[6]=7
AMlvarValue[7]=10
AMlvarValue[8]=0
AMlvarValue[9]=8
AMlvarValue[10]=0
AMlvarValue[11]=0
AMlvarValue[12]=0
AMlvarValue[13]=0
AMlvarValue[14]=100
AMlvarValue[15]=0
AMlvarValue[16]="none"

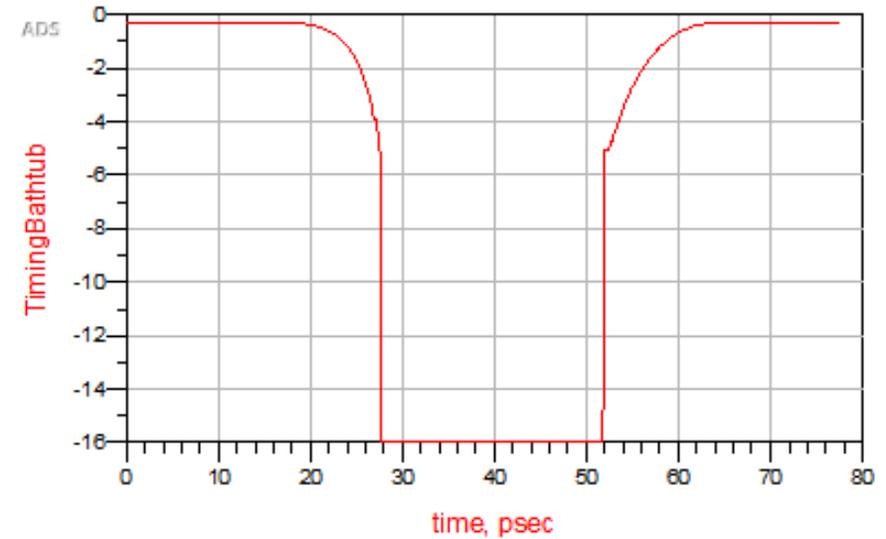
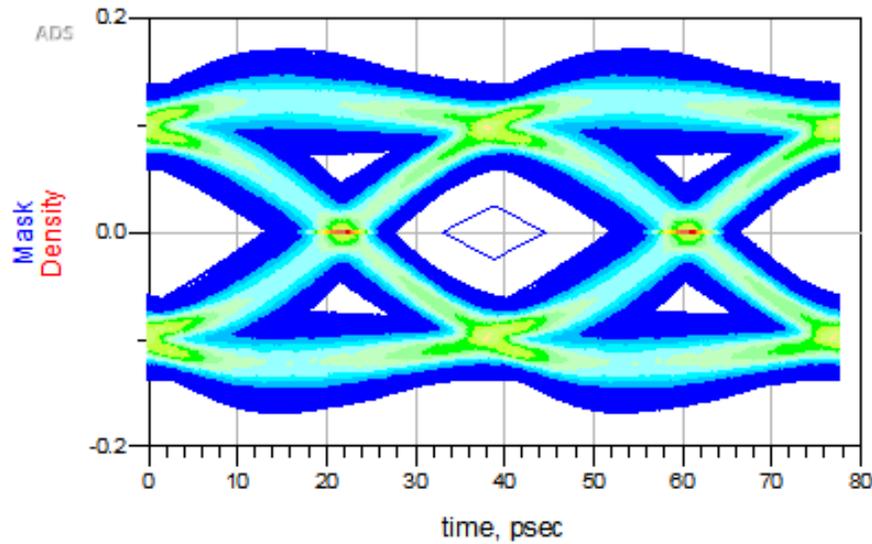


ChannelSim
ChannelSim1
NumberOfBits=1000000
ToleranceMode=Auto
EnforcePassivity=yes

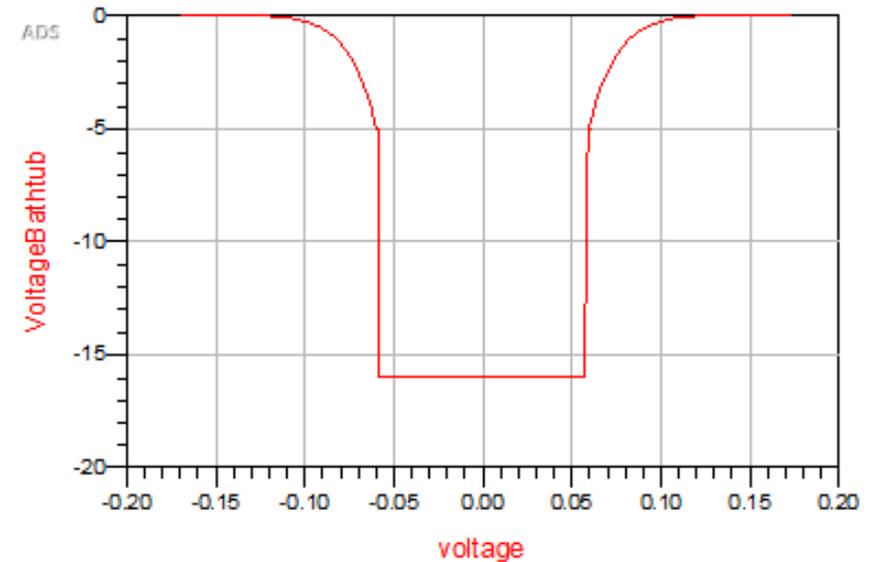


Rx_AMI
Rx_AMI2
ComponentName="ibm_hss15c2c_cu032_rx_nc"
PinName="2p"
ModelName="ibm_hss15c2c_cu032_rx_nc"
SetAllData=yes
DataTypeSelector=Typ
UsePkg=yes
CacType=Typ
AMlvarName[1]=Ignore_Bits
AMlvarName[2]=Max_Init_Aggressors
AMlvarName[3]=Init_Returns_Impulse
AMlvarName[4]=GetWave_Exists
AMlvarName[5]=Use_Init_Output
AMlvarName[6]=Rx_Clock_PDF
AMlvarName[7]=Rx_Receiver_Sensitivity
AMlvarName[8]=baud
AMlvarName[9]=sjrx
AMlvarName[10]=sjrx_freq
AMlvarName[11]=anvga
AMlvarName[12]=gain
AMlvarName[13]=negz
AMlvarName[14]=VTR
AMlvarName[15]=HtLimit
AMlvarName[16]=Fc1667
AMlvarName[17]=rxcte
AMlvarName[18]=rxic
AMlvarName[19]=rxh
AMlvarName[20]=Rx_RJ
AMlvarName[21]=agcgain
AMlvarName[22]=agcmax
AMlvarName[23]=agcmin
AMlvarName[24]=agclev
AMlvarName[25]=rotlin
AMlvarName[26]=ndfe
AMlvarName[27]=dfelimit
AMlvarName[28]=freqofs
AMlvarName[29]=dfeadaptoff
AMlvarName[30]=dfeoff
AMlvarName[31]=wavecap
AMlvarName[32]=ADS_VendorID
AMlvarValue[7]=0.013
AMlvarValue[8]=1.25e9
AMlvarValue[9]=0.05
AMlvarValue[10]=1.54e8
AMlvarValue[11]=2.0335e-3
AMlvarValue[12]="mid"
AMlvarValue[13]=0
AMlvarValue[14]=1.05
AMlvarValue[15]=3
AMlvarValue[16]=0
AMlvarValue[17]="ibm/hss15c2c/cu032/ic_rx_ncAVTR1_05negzen0gain_dec255.cte:ami"
AMlvarValue[18]="ibm/hss15c2c/cu032/icAVTR1_05negzen0gain_dec255peak_dec0_normn.s4p"
AMlvarValue[19]=0
AMlvarValue[20]=420e-15
AMlvarValue[21]=0.0

Statistical Eye: 25Gbps 1 Million Bit-By-Bit Simulation

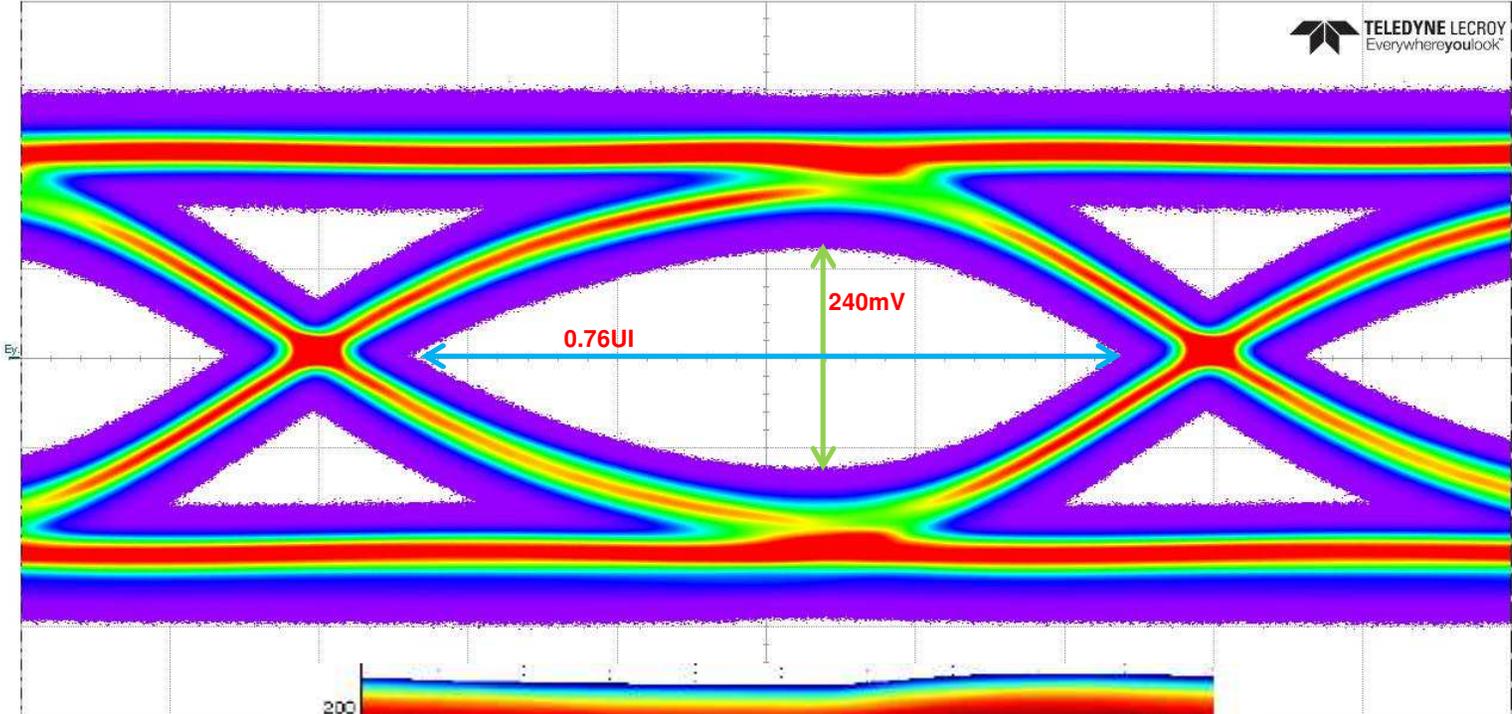


index	...HeightAtBER)	...WidthAtBER)
0.0000	121.0 m	24.59 p



Statistical Eye: 6.25Gbps Measurement vs. Simulation

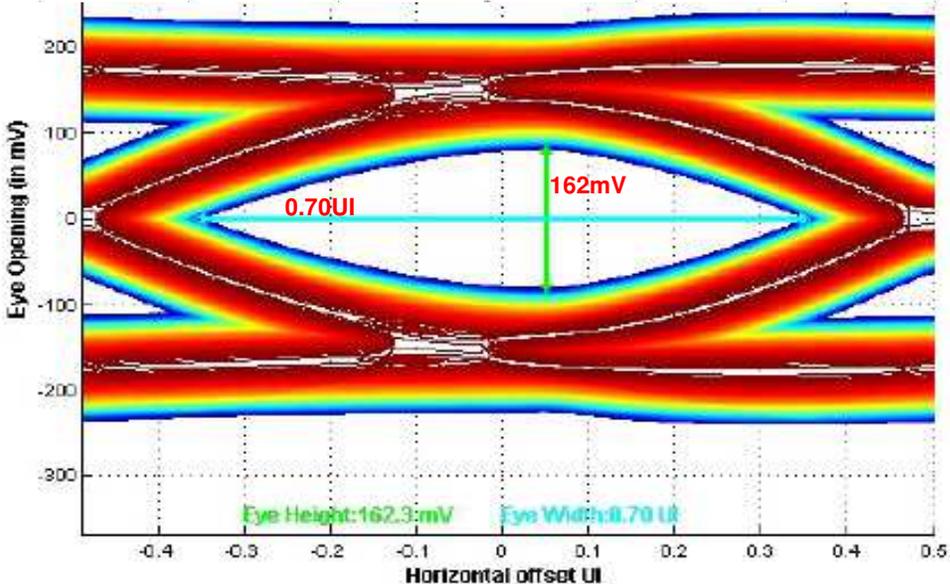
Measurement



Eye
100 mV/div
26.7 ps/div
1.91698 G#
L
t
Δy

Timebase 600 ns Trigger C4:DC
5.00 ps/div Auto 31 mV
2.00 MS 40 GS/s Edge Positive
X1= -53.5 ps ΔX= 267.0 ps
X2= 213.6 ps 1/ΔX= 3.745 GHz

Simulation
(from LinkEye)



Eye Height: 162.3 mV Eye Width: 0.70 UI

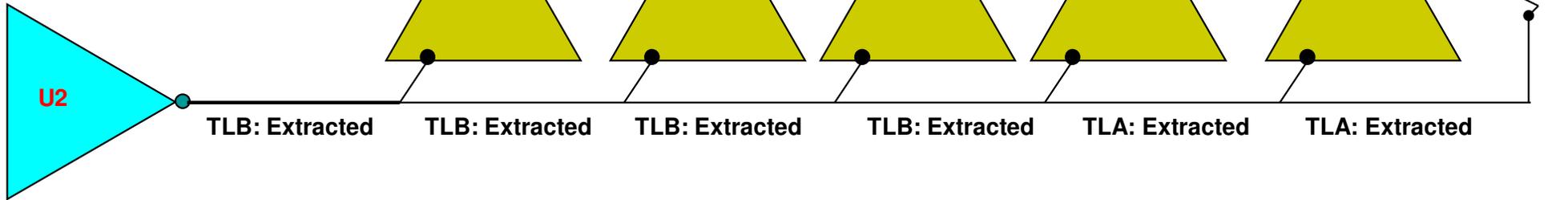
DDR4 Example

600MHz DDR4 Post-Layout Address Path

TLB		
Width	Layer	Zo
4.25 mil	14	40

Micron MT40A512M16LY
lbis model: z11b.ibs
Package: z11b_96ball_pkg
Input Model: INPUT

Xilinx



Model: HP_SSTL12_DCI_M_OUT40

Corner: Slow-Slow

Package: xczu7eg_ffvc1156

Vref = 0.600V

MT40A512M16JY	
1200MHz, 2400	AC100
VIHAC	700
VIHDC	675
VREF	600
VILDC	525
VILAC	500
tIS	55+
tIH	80+

Clock and Address Extracted Nets

Nets to Extract:

DDR_CK0_N
DDR_CK0_P

DDR_PARITY
DDR_ADD(11)
DDR_ADD(2)
DDR_ADD(8)
DDR_ADD(0)
DDR_ADD(6)
DDR_ADD(4)
DDR_BA0
DDR_ADD(10)
DDR_BG0
DDR_ACT_L
DDR_WE_L
DDR_ODT0
DDR_CKE0

GND

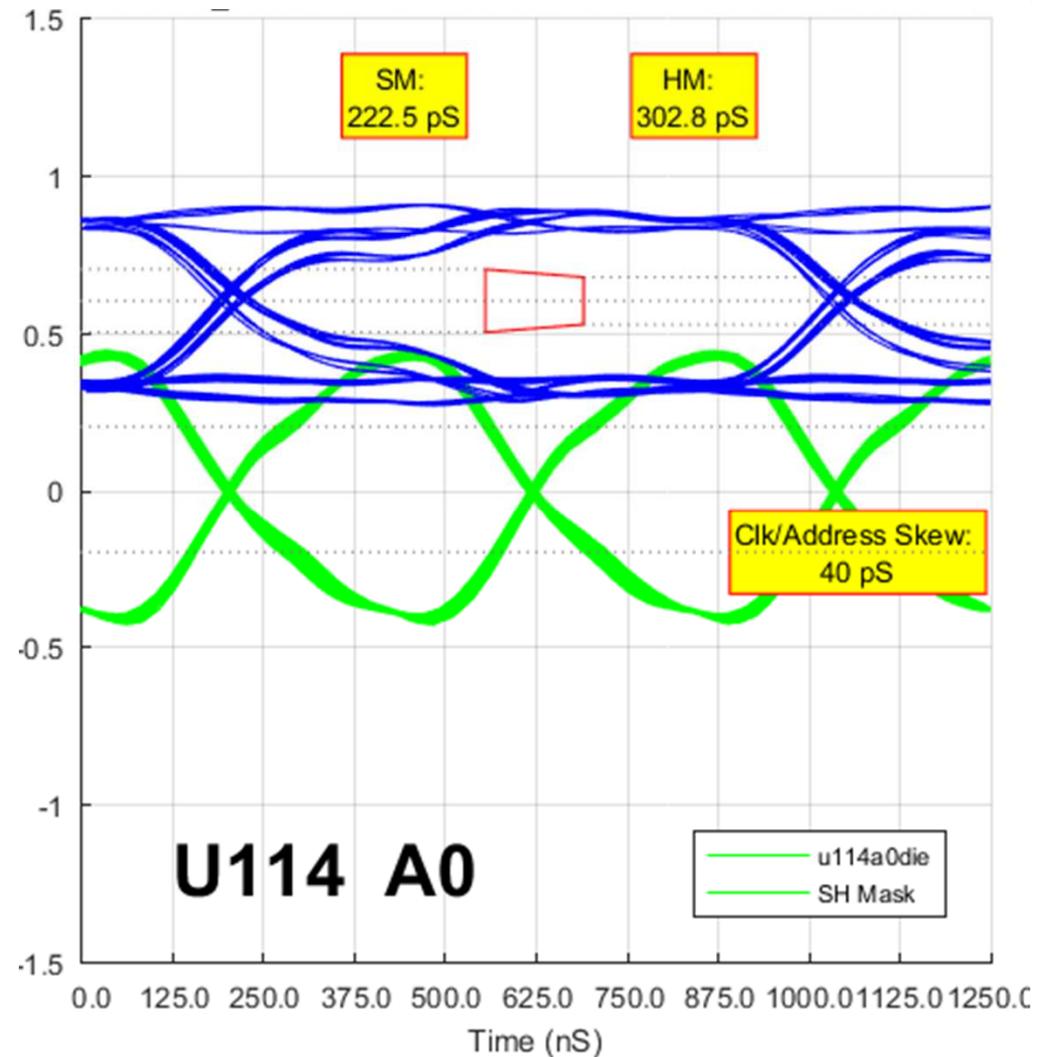
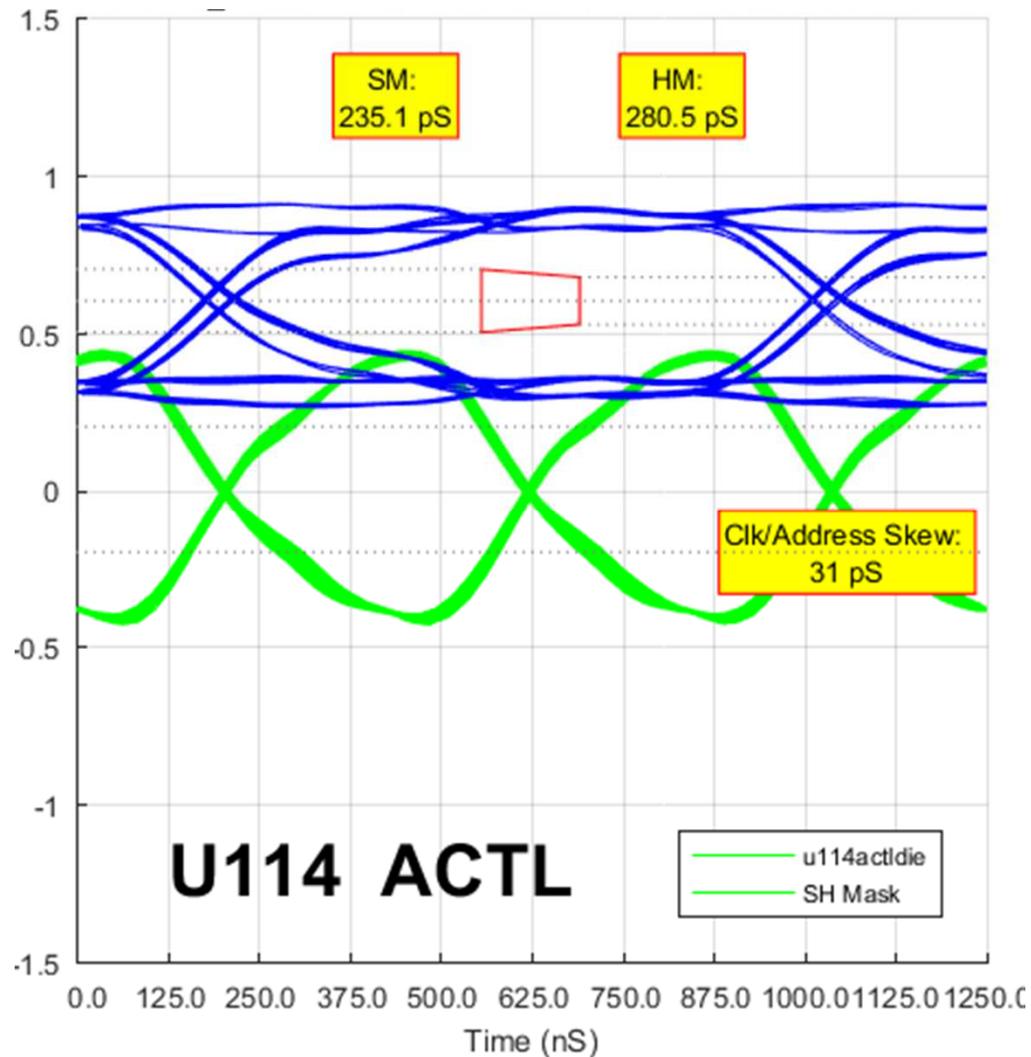


Summary: PS DDR4x5 Post-Layout Clock/Address HP_SSTL12_DCI_M_OUT40

Tx	Rx	Net	Corner	Setup Margin	Hold Margin	Overshoot	Undershoot	Skew	Status
U2	U114	ACTL	Slow-Slow	235.1 pS	280.5 pS	-0.589	-0.562	-30.5 pS	Pass
U2	U114	A0	Slow-Slow	222.5 pS	302.8 pS	-0.595	-0.568	-39.9 pS	Pass
U2	U114	A2	Slow-Slow	205.9 pS	309.1 pS	-0.591	-0.568	-46.8 pS	Pass
U2	U114	A4	Slow-Slow	218.6 pS	307.1 pS	-0.591	-0.562	-43.7 pS	Pass
U2	U114	A6	Slow-Slow	168.5 pS	306.9 pS	-0.576	-0.545	-49.7 pS	Pass
U2	U114	A8	Slow-Slow	178.3 pS	307.0 pS	-0.591	-0.564	-53.5 pS	Pass
U2	U114	A10	Slow-Slow	210.6 pS	308.1 pS	-0.573	-0.548	-51.4 pS	Pass
U2	U114	A11	Slow-Slow	178.1 pS	306.5 pS	-0.598	-0.564	-55.4 pS	Pass
U2	U114	BA0	Slow-Slow	224.7 pS	294.4 pS	-0.596	-0.564	-24.3 pS	Pass
U2	U114	BG0	Slow-Slow	214.2 pS	290.6 pS	-0.583	-0.559	-36.2 pS	Pass
U2	U114	CKE0	Slow-Slow	239.2 pS	263.2 pS	-0.597	-0.569	-24.2 pS	Pass
U2	U114	ODT0	Slow-Slow	243.9 pS	276.8 pS	-0.593	-0.564	-35.7 pS	Pass
U2	U114	PARITY	Slow-Slow	230.7 pS	271.8 pS	-0.596	-0.571	-21.9 pS	Pass
U2	U114	WEL	Slow-Slow	248.8 pS	269.9 pS	-0.588	-0.568	-10.6 pS	Pass
U2	U111	ACTL	Slow-Slow	263.4 pS	261.4 pS	-0.578	-0.566	-9.8 pS	Pass
U2	U111	A0	Slow-Slow	238.8 pS	288.0 pS	-0.594	-0.569	-38.0 pS	Pass
U2	U111	A2	Slow-Slow	234.5 pS	296.8 pS	-0.586	-0.565	-41.9 pS	Pass
U2	U111	A4	Slow-Slow	233.6 pS	292.2 pS	-0.582	-0.562	-44.8 pS	Pass
U2	U111	A6	Slow-Slow	243.1 pS	300.8 pS	-0.580	-0.558	-44.7 pS	Pass
U2	U111	A8	Slow-Slow	248.3 pS	300.6 pS	-0.596	-0.576	-36.9 pS	Pass
U2	U111	A10	Slow-Slow	235.4 pS	294.7 pS	-0.583	-0.556	-48.8 pS	Pass
U2	U111	A11	Slow-Slow	248.3 pS	302.6 pS	-0.599	-0.572	-33.0 pS	Pass
U2	U111	BA0	Slow-Slow	264.0 pS	275.7 pS	-0.599	-0.575	-15.0 pS	Pass
U2	U111	BG0	Slow-Slow	262.9 pS	273.4 pS	-0.590	-0.566	-21.6 pS	Pass
U2	U111	CKE0	Slow-Slow	292.8 pS	249.0 pS	-0.593	-0.573	7.5 pS	Pass
U2	U111	ODT0	Slow-Slow	269.8 pS	258.8 pS	-0.582	-0.571	-6.5 pS	Pass
U2	U111	PARITY	Slow-Slow	269.1 pS	265.5 pS	-0.606	-0.587	-5.0 pS	Pass
U2	U111	WEL	Slow-Slow	284.7 pS	252.2 pS	-0.601	-0.577	4.7 pS	Pass
U2	U110	ACTL	Slow-Slow	304.5 pS	263.6 pS	-0.568	-0.556	17.4 pS	Pass
U2	U110	A0	Slow-Slow	275.4 pS	296.2 pS	-0.577	-0.561	-16.0 pS	Pass
U2	U110	A2	Slow-Slow	268.1 pS	308.2 pS	-0.572	-0.552	-25.5 pS	Pass
U2	U110	A4	Slow-Slow	275.0 pS	303.2 pS	-0.571	-0.557	-19.7 pS	Pass
U2	U110	A6	Slow-Slow	263.0 pS	303.0 pS	-0.548	-0.532	-33.7 pS	Pass
U2	U110	A8	Slow-Slow	269.4 pS	302.2 pS	-0.570	-0.548	-25.9 pS	Pass
U2	U110	A10	Slow-Slow	273.0 pS	304.7 pS	-0.571	-0.560	-22.9 pS	Pass
U2	U110	A11	Slow-Slow	270.4 pS	303.2 pS	-0.587	-0.559	-26.6 pS	Pass

Tx	Rx	Net	Corner	Setup Margin	Hold Margin	Overshoot	Undershoot	Skew	Status
U2	U110	BA0	Slow-Slow	295.2 pS	273.4 pS	-0.579	-0.552	-0.9 pS	Pass
U2	U110	BG0	Slow-Slow	294.0 pS	269.9 pS	-0.597	-0.576	-4.0 pS	Pass
U2	U110	CKE0	Slow-Slow	314.6 pS	249.1 pS	-0.610	-0.587	24.5 pS	Pass
U2	U110	ODT0	Slow-Slow	299.8 pS	262.5 pS	-0.579	-0.572	16.2 pS	Pass
U2	U110	PARITY	Slow-Slow	304.4 pS	268.1 pS	-0.586	-0.566	17.0 pS	Pass
U2	U110	WEL	Slow-Slow	316.1 pS	256.9 pS	-0.596	-0.578	24.6 pS	Pass
U2	U112	ACTL	Slow-Slow	291.5 pS	249.6 pS	-0.605	-0.571	25.1 pS	Pass
U2	U112	A0	Slow-Slow	260.1 pS	272.6 pS	-0.606	-0.581	-9.8 pS	Pass
U2	U112	A2	Slow-Slow	256.8 pS	288.0 pS	-0.605	-0.575	-22.1 pS	Pass
U2	U112	A4	Slow-Slow	259.0 pS	272.0 pS	-0.598	-0.581	-16.1 pS	Pass
U2	U112	A6	Slow-Slow	246.5 pS	280.1 pS	-0.594	-0.571	-26.8 pS	Pass
U2	U112	A8	Slow-Slow	258.3 pS	295.1 pS	-0.605	-0.578	-24.4 pS	Pass
U2	U112	A10	Slow-Slow	262.7 pS	279.1 pS	-0.606	-0.582	-17.4 pS	Pass
U2	U112	A11	Slow-Slow	257.4 pS	306.2 pS	-0.610	-0.579	-27.9 pS	Pass
U2	U112	BA0	Slow-Slow	283.7 pS	273.3 pS	-0.613	-0.583	4.1 pS	Pass
U2	U112	BG0	Slow-Slow	284.5 pS	276.5 pS	-0.621	-0.593	-3.9 pS	Pass
U2	U112	CKE0	Slow-Slow	323.0 pS	247.4 pS	-0.628	-0.603	35.1 pS	Pass
U2	U112	ODT0	Slow-Slow	295.8 pS	250.6 pS	-0.625	-0.598	25.6 pS	Pass
U2	U112	PARITY	Slow-Slow	301.3 pS	262.9 pS	-0.615	-0.579	22.4 pS	Pass
U2	U112	WEL	Slow-Slow	313.2 pS	253.9 pS	-0.618	-0.590	25.8 pS	Pass
U2	U113	ACTL	Slow-Slow	324.3 pS	253.0 pS	-0.618	-0.612	24.6 pS	Pass
U2	U113	A0	Slow-Slow	290.8 pS	286.2 pS	-0.596	-0.605	-3.9 pS	Pass
U2	U113	A2	Slow-Slow	282.4 pS	297.3 pS	-0.592	-0.607	-14.4 pS	Pass
U2	U113	A4	Slow-Slow	289.3 pS	289.5 pS	-0.589	-0.607	-8.7 pS	Pass
U2	U113	A6	Slow-Slow	276.6 pS	285.4 pS	-0.599	-0.608	-9.2 pS	Pass
U2	U113	A8	Slow-Slow	278.4 pS	291.7 pS	-0.610	-0.620	-9.8 pS	Pass
U2	U113	A10	Slow-Slow	292.8 pS	299.0 pS	-0.589	-0.608	-10.7 pS	Pass
U2	U113	A11	Slow-Slow	272.3 pS	295.4 pS	-0.610	-0.620	-15.0 pS	Pass
U2	U113	BA0	Slow-Slow	299.5 pS	274.3 pS	-0.612	-0.616	10.5 pS	Pass
U2	U113	BG0	Slow-Slow	297.9 pS	282.8 pS	-0.616	-0.623	3.4 pS	Pass
U2	U113	CKE0	Slow-Slow	333.8 pS	246.2 pS	-0.654	-0.633	42.4 pS	Pass
U2	U113	ODT0	Slow-Slow	325.7 pS	252.5 pS	-0.639	-0.627	28.5 pS	Pass
U2	U113	PARITY	Slow-Slow	311.4 pS	264.2 pS	-0.625	-0.620	19.8 pS	Pass
U2	U113	WEL	Slow-Slow	327.0 pS	257.0 pS	-0.620	-0.629	32.4 pS	Pass

PS DDR4x5 Post-Layout Clock/Address HP_SSTL12_DCI_M_OUT40



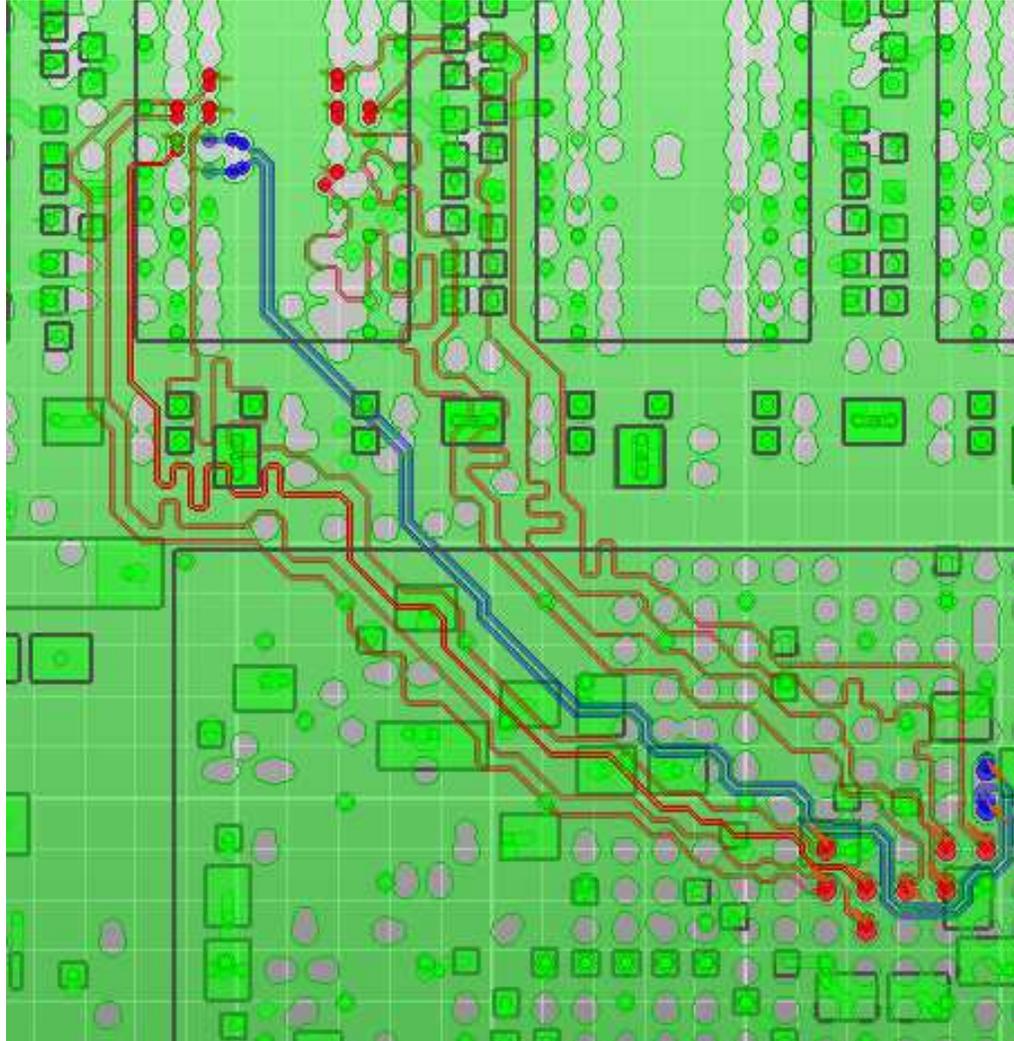
DQ and DQS Extracted Nets

Nets to Extract:

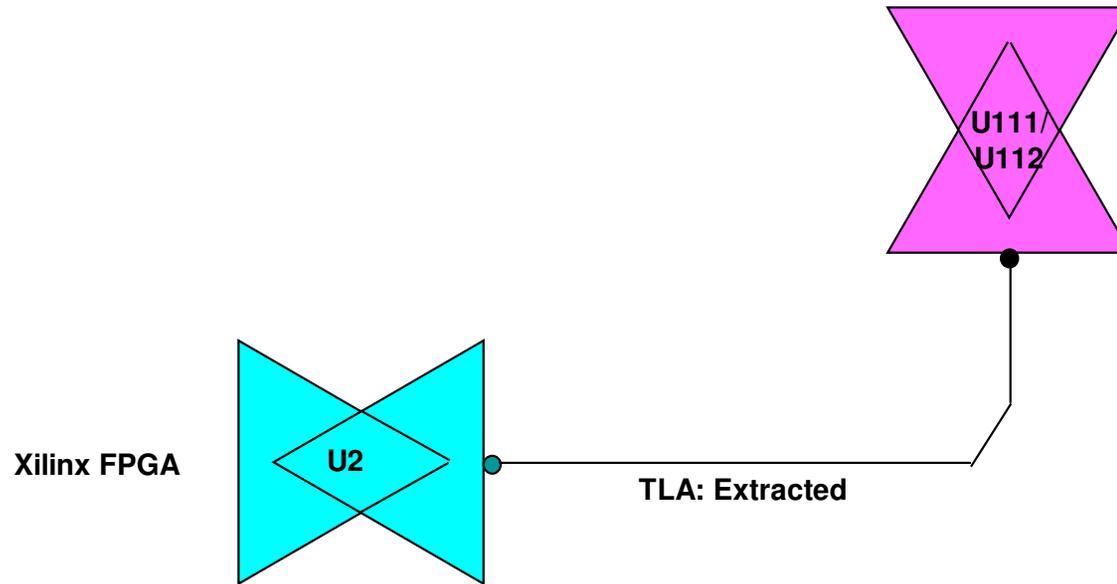
DDR_DQS2_N
DDR_DQS2_P

DDR_DQ(16)
DDR_DQ(17)
DDR_DQ(18)
DDR_DQ(19)
DDR_DQ(20)
DDR_DQ(21)
DDR_DQ(22)
DDR_DQ(23)

GND



1200MHz Post-Layout PL DDR4 Data Path



Micron MT40A512M16LY
Ibis Model: z11b.ibs
Package: z11b_96ball_pkg
Write Model: DQ_IN_ODT60_3200
Read Model: DQ_40_3200

Write Model: HP_POD12_DCI_F_OUT40
Read Model: HP_POD12_DCI_F_OUT40_IN40
Corner: Slow-Slow
Package: xczu7eg_ffvc1156
Vref = 0.60V

MT40A512M16JY	
1200MHz, 2400	AC100
VIHAC	860
VIHDC	860
VREF	Varies
VILDC	740
VILAC	740
tDS	42+
tDH	42+

Summary: DDR4 Post-Layout Write and Read

Dir	Tx	Rx	Net	Corner	EyeHeight	EyeWidth	PulseWidth	RxMaskOff	Max SRR	Min SRR	Max SRF	Min SRF	OverShoot	UnderShoot	Status
Write	U2	U111	DQ16	Slow-Slow	533.2	371.8	416.5	4.9	5.7	4.9	5.7	4.9	-0.398	-0.694	Pass
Write	U2	U111	DQ17	Slow-Slow	589.2	375.4	416.5	2.2	5.6	4.9	5.7	4.9	-0.406	-0.709	Pass
Write	U2	U111	DQ18	Slow-Slow	531.5	370.7	416.4	5.4	6.1	4.8	6.2	4.9	-0.401	-0.682	Pass
Write	U2	U111	DQ19	Slow-Slow	536.8	370.4	416.4	5.3	6.0	4.9	6.1	4.9	-0.404	-0.684	Pass
Write	U2	U111	DQ20	Slow-Slow	537.8	373.5	416.5	9.6	6.0	5.0	6.1	5.0	-0.394	-0.695	Pass
Write	U2	U111	DQ21	Slow-Slow	561.4	375.2	416.5	7.1	5.5	4.7	5.5	4.8	-0.400	-0.709	Pass
Write	U2	U111	DQ22	Slow-Slow	500.2	377.8	416.5	14.3	6.2	5.0	6.2	5.0	-0.385	-0.686	Pass
Write	U2	U111	DQ23	Slow-Slow	451.8	365.3	416.4	24.2	6.5	4.1	6.6	4.2	-0.367	-0.660	Pass
Read	U111	U2	DQ16	Slow-Slow	525.4	370.7	416.3	6.8	4.5	3.4	4.5	3.3	-0.424	-0.845	Pass
Read	U111	U2	DQ17	Slow-Slow	552.9	375.4	416.4	0.4	4.3	3.5	4.4	3.5	-0.442	-0.866	Pass
Read	U111	U2	DQ18	Slow-Slow	533.7	373.8	416.4	5.7	4.3	3.8	4.3	3.7	-0.440	-0.869	Pass
Read	U111	U2	DQ19	Slow-Slow	533.0	372.0	416.4	4.7	4.2	3.7	4.2	3.6	-0.436	-0.864	Pass
Read	U111	U2	DQ20	Slow-Slow	526.1	370.5	416.4	12.0	4.4	3.4	4.4	3.3	-0.428	-0.849	Pass
Read	U111	U2	DQ21	Slow-Slow	533.8	370.0	416.3	9.7	4.5	3.4	4.5	3.3	-0.425	-0.848	Pass
Read	U111	U2	DQ22	Slow-Slow	524.1	370.9	416.3	13.4	4.2	3.5	4.2	3.5	-0.440	-0.869	Pass
Read	U111	U2	DQ23	Slow-Slow	495.5	366.6	416.2	24.0	4.5	3.1	4.5	3.1	-0.418	-0.838	Pass
Write	U2	U112	DQ40	Slow-Slow	686.8	356.2	417.0	4.3	6.1	3.9	6.1	3.9	-0.355	-0.647	Pass
Write	U2	U112	DQ41	Slow-Slow	653.3	358.1	417.0	12.0	6.5	3.7	6.4	3.7	-0.343	-0.632	Pass
Write	U2	U112	DQ42	Slow-Slow	702.9	353.8	416.9	10.8	5.8	4.6	5.8	4.5	-0.374	-0.677	Pass
Write	U2	U112	DQ43	Slow-Slow	700.3	353.1	416.8	10.5	5.9	4.6	6.0	4.6	-0.372	-0.673	Pass
Write	U2	U112	DQ44	Slow-Slow	688.3	351.6	417.1	2.0	5.8	3.8	5.8	3.8	-0.357	-0.653	Pass
Write	U2	U112	DQ45	Slow-Slow	655.2	352.5	417.1	5.9	5.9	3.8	5.9	3.8	-0.344	-0.632	Pass
Write	U2	U112	DQ46	Slow-Slow	674.6	357.2	416.9	4.1	6.3	4.3	6.2	4.2	-0.357	-0.653	Pass
Write	U2	U112	DQ47	Slow-Slow	665.7	359.4	417.1	10.3	6.6	3.6	6.7	3.6	-0.342	-0.629	Pass
Read	U112	U2	DQ40	Slow-Slow	589.5	366.6	416.4	7.6	4.3	3.1	4.3	3.1	-0.430	-0.869	Pass
Read	U112	U2	DQ41	Slow-Slow	572.4	368.2	416.4	15.2	4.4	3.1	4.4	3.2	-0.430	-0.868	Pass
Read	U112	U2	DQ42	Slow-Slow	605.1	372.0	416.4	7.6	4.3	3.5	4.3	3.5	-0.439	-0.875	Pass
Read	U112	U2	DQ43	Slow-Slow	596.4	371.3	416.3	8.1	4.4	3.7	4.4	3.7	-0.440	-0.875	Pass
Read	U112	U2	DQ44	Slow-Slow	588.5	364.8	416.4	4.6	4.4	3.0	4.4	3.0	-0.427	-0.864	Pass
Read	U112	U2	DQ45	Slow-Slow	565.7	367.4	416.3	7.5	4.3	3.2	4.3	3.1	-0.426	-0.865	Pass
Read	U112	U2	DQ46	Slow-Slow	576.0	368.6	416.4	7.2	4.2	3.4	4.2	3.4	-0.435	-0.874	Pass
Read	U112	U2	DQ47	Slow-Slow	574.4	361.1	416.4	14.0	4.3	2.9	4.3	2.9	-0.429	-0.862	Pass

DDR4 Post-Layout U2-to-U111

DQS/DQ HP_PO D12 DCI_F_OUT40

